ZURG (13.3" AMD)

AMD Lucienne &Cazenne

203016-1

Functional Data sheet	**56177**
EDS	**56417**
Motherboard Design Guide	**56178**
Motherboard Schematic Checklist	**56179**
PPOG	**56465**

VDDCR	**1V_VDDCR_CPU**
VDDCR_SOC	**1V_VDDCR_SOC**
VDDIO_MEM_S3	**1D2V_S3**
VDDP	**0D75V_VDDP_S0**
VDDP_S5	**0D75V_VDDP_S5**
VDD18	**1D8V_S0**
VDD_18_S5	**1D8V_S5**
VDD_33	**3D3V_S0**
VDD_33_S5	**3D3V_S5**
VDDIO_AUDIO	**1D8V_S5**
VDDBT_RTC_G	**3D3V_VDDBT_RTC**
VDDIO_VPH	**VDDIO_VPH**

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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***

Size	Document Number	Rev
A4	**13" CS ZURG Lucienne**	**-1**

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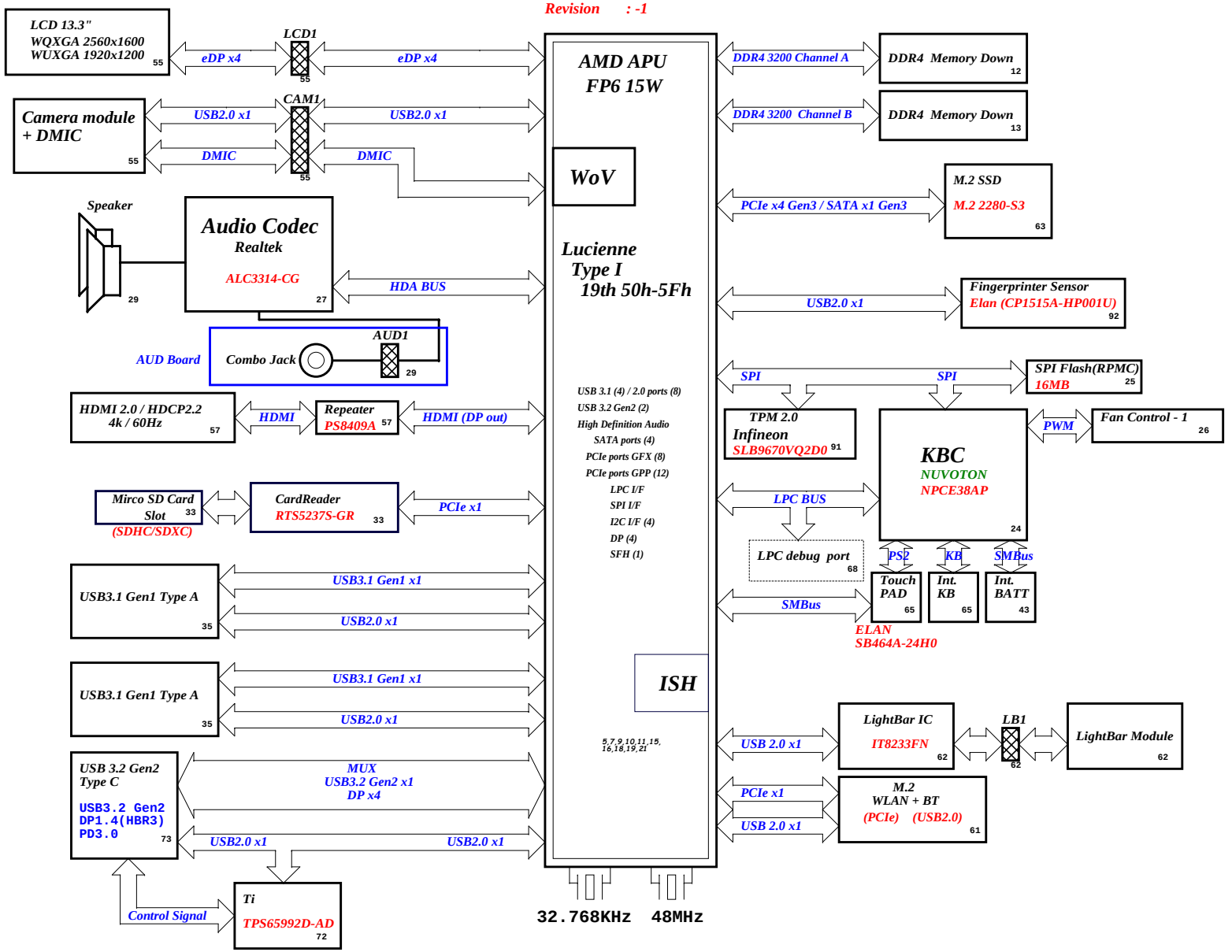
Toy Story CS 13" AMD
Lucienne & Cezanne

Project code :
ZURG 1.0 UMA-->4PD0NE010001(停用)
ZURG 1.1 CZN UMA-->4PD0NE01A001

PCB P/N : 203016
Revision : -1



CHARGER ISL9538BHRTZ-T	44
INPUTS	OUTPUTS
AD+ BT+ USB_ADT	19V_DCBATOUT

SYSTEM DC/DC SY8388BRHC (3D3V) SY8388CRHC (5V)	45
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_S5 3D3V_AUX_S5 5V_S5 5V_AUX_S5

CPU DC/DC RT3662AMGQW	46~50
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VDDCR_CPU 1V_VDDCR_SOC

SYSTEM DC/DC RT8231AGQW (1D2V)	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D2V_S3 0D6V_VREF_S0

SYSTEM LDO G946F11U (2D5V)	51
INPUTS	OUTPUTS
3D3V_S5	2D5V_S3

SYSTEM DC/DC G2822DRC1U (0D75V)	52
INPUTS	OUTPUTS
3D3V_S5	0D75V_VDDP_S5

SYSTEM LDO G2822DRC1U (0D75V)	52
INPUTS	OUTPUTS
5V_S5	0D75V_VDDP_S0

SYSTEM DC/DC G5335DQZ1U (1D8V)	53
INPUTS	OUTPUTS
19V_DCBATOUT	1D8V_S5

Load Switches G2898KD1U (3D3V/5V) G2898KD1U (1D8V)	40
INPUTS	OUTPUTS
5V_S5 3D3V_S5 1D8V_S5	5V_S0 3D3V_S0 1D8V_S0

PCB LAYER

L1 : TOP
L2 : GND
L3 : Signal
L4 : GND/PWR
L5 : Signal
L6 : Signal
L7 : GND
L8 : Signal
L9 : GND/PWR
L10 : BOTTOM

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A01

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Title: Block Diagram
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PCIe (GFX)

P_GFX port	Device	CLKREQ#
0	N/A	
1	N/A	
2	N/A	
3	N/A	
4	N/A	
5	N/A	
6	N/A	
7	N/A	

PCIe (GPP)

P_GPP port	Device	CLKREQ#
0	M.2 SSD	0
1	M.2 SSD	
2	M.2 SSD	
3	M.2 SSD	
4	CR	4
5	N/A	
6	N/A	
7	WIFI	1
8	N/A	
9	N/A	
10	N/A	
11	N/A	

SATA

Port	Device
0	N/A
1	M.2 SSD
2	N/A
3	N/A

CPU1B

PCIE

GFX & GPP, 85Ω

G13	P_GFX_RXP0	P_GFX_TXP0	F4
F13	P_GFX_RXN0	P_GFX_TXN0	F2
J14	P_GFX_RXP1	P_GFX_TXP1	F3
H14	P_GFX_RXN1	P_GFX_TXN1	E4
G15	P_GFX_RXP2	P_GFX_TXP2	E1
F15	P_GFX_RXN2	P_GFX_TXN2	C1
J15	P_GFX_RXP3	P_GFX_TXP3	D5
K15	P_GFX_RXN3	P_GFX_TXN3	E6
H16	P_GFX_RXP4	P_GFX_TXP4	C6
J16	P_GFX_RXN4	P_GFX_TXN4	D6
F18	P_GFX_RXP5	P_GFX_TXP5	B6
G18	P_GFX_RXN5	P_GFX_TXN5	C7
J18	P_GFX_RXP6	P_GFX_TXP6	D8
K18	P_GFX_RXN6	P_GFX_TXN6	B8
H19	P_GFX_RXP7	P_GFX_TXP7	C8
G19	P_GFX_RXN7	P_GFX_TXN7	A8

M.2 SSD

63	SSD_PCIE_RX_P3	G11	P_GPP_RXP0	P_GPP_TXP0	L3	SSD_PCIE_TX_P3	C311 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_P3 63
63	SSD_PCIE_RX_N3	F11	P_GPP_RXN0	P_GPP_TXN0	L1	SSD_PCIE_TX_N3	C312 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_N3 63
63	SSD_PCIE_RX_P2	J10	P_GPP_RXP1	P_GPP_TXP1	L4	SSD_PCIE_TX_P2	C309 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_P2 63
63	SSD_PCIE_RX_N2	H10	P_GPP_RXN1	P_GPP_TXN1	L2	SSD_PCIE_TX_N2	C310 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_N2 63
63	SSD_PCIE_RX_P1	G8	P_GPP_RXP2/SATA0_RXP	P_GPP_TXP2/SATA0_TXP	M4	SSD_PCIE_TX_P1	C307 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_P1 63
63	SSD_PCIE_RX_N1	F8	P_GPP_RXN2/SATA0_RXN	P_GPP_TXN2/SATA0_TXN	M2	SSD_PCIE_TX_N1	C308 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_N1 63
63	SSD_PCIE_RX_P0	G6	P_GPP_RXP3/SATA1_RXP	P_GPP_TXP3/SATA1_TXP	N3	SSD_PCIE_TX_P0	C305 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_P0 63
63	SSD_PCIE_RX_N0	F7	P_GPP_RXN3/SATA1_RXN	P_GPP_TXN3/SATA1_TXN	N1	SSD_PCIE_TX_N0	C306 1	SCD22U10V2KX-L1-GP	SSD_PCIE_TX_CON_N0 63

M.2 SSD (Gen3)

CR

33	CARD_PCIE_RX_P	M9	P_GPP_RXP4	P_GPP_TXP4	T2	CARD_PCIE_TX_P_C	C301 1	SCD1U16V2KX-L-GP	CARD_PCIE_TX_P 33
33	CARD_PCIE_RX_N	M8	P_GPP_RXN4	P_GPP_TXN4	T4	CARD_PCIE_TX_N_C	C302 1	SCD1U16V2KX-L-GP	CARD_PCIE_TX_N 33

CR (Gen1)

		L7	P_GPP_RXP5	P_GPP_TXP5	R1				
		L6	P_GPP_RXN5	P_GPP_TXN5	R3				
		K7	P_GPP_RXP6	P_GPP_TXP6	P2				
		K8	P_GPP_RXN6	P_GPP_TXN6	P4				

WIFI

61	WLAN_PCIE_RX_P	H6	P_GPP_RXP7	P_GPP_TXP7	N2	WLAN_PCIE_TX_P	C303 1	Do Not Stuff	WLAN_PCIE_TX_CON_P 61
61	WLAN_PCIE_RX_N	H7	P_GPP_RXN7	P_GPP_TXN7	N4	WLAN_PCIE_TX_N	C304 1	Do Not Stuff	WLAN_PCIE_TX_CON_N 61

SD
SD

WIFI (Gen1)

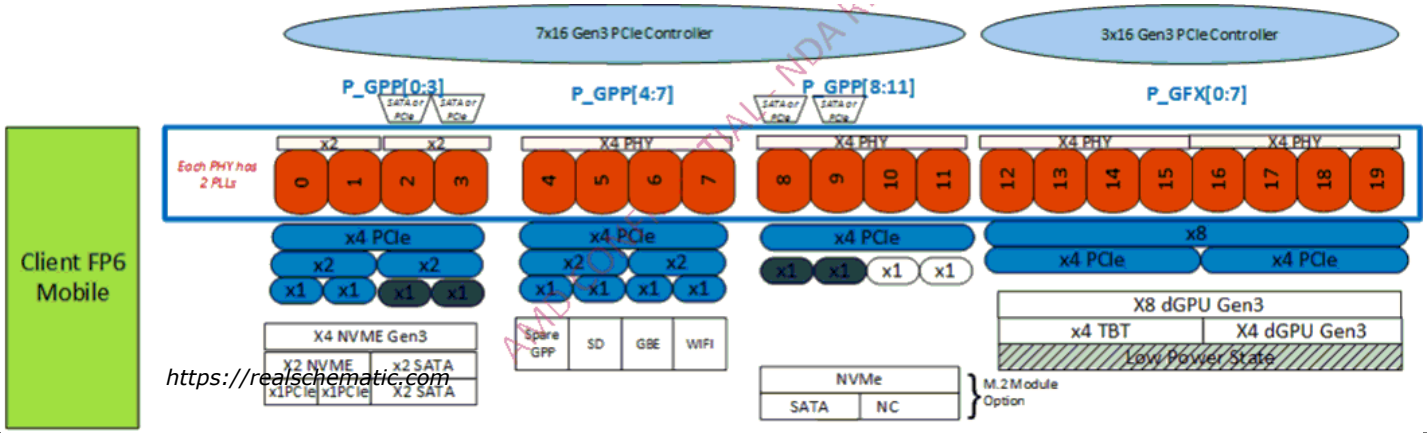
		L9	P_GPP_RXP8/SATA2_RXP	P_GPP_TXP8/SATA2_TXP	K2				
		L10	P_GPP_RXN8/SATA2_RXN	P_GPP_TXN8/SATA2_TXN	K4				
		K11	P_GPP_RXP9/SATA3_RXP	P_GPP_TXP9/SATA3_TXP	J4				
		J11	P_GPP_RXN9/SATA3_RXN	P_GPP_TXN9/SATA3_TXN	J2				
		J12	P_GPP_RXP10	P_GPP_TXP10	H3				
		H12	P_GPP_RXN10	P_GPP_TXN10	H1				
		J13	P_GPP_RXP11	P_GPP_TXP11	H4				
		K13	P_GPP_RXN11	P_GPP_TXN11	H2				

FP6 REV 0.92
PART 2 OF 13

RENOIR-FP6-GP
CPU

1st = L86038-001
2nd = L86038-001
3rd = L86288-001
4th = L86288-001

Note : #56179 v.0.5
Recommended value for supporting both PCIe Gen 2.0 and Gen 3.0 operation is 220 nF ±10%.
Recommended value for supporting PCIe Gen 3.0 operation only is 220 nF ±10%.
Recommended value for supporting PCIe Gen 2.0 operation only is 100 nF ±10%.
PCIE Gen3 cap value apply to Gen1 (by AMD FAE mail-20190604)



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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (PCIE/SATA)**

Size	Document Number	Rev
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5 4 3 2 1

D

C

B

A

TBD

A01

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (Reserved)

Size	Document Number	Rev
A4	**13" CS ZURG Lucienne**	-1

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DDR4
Channel A to DRAM Down

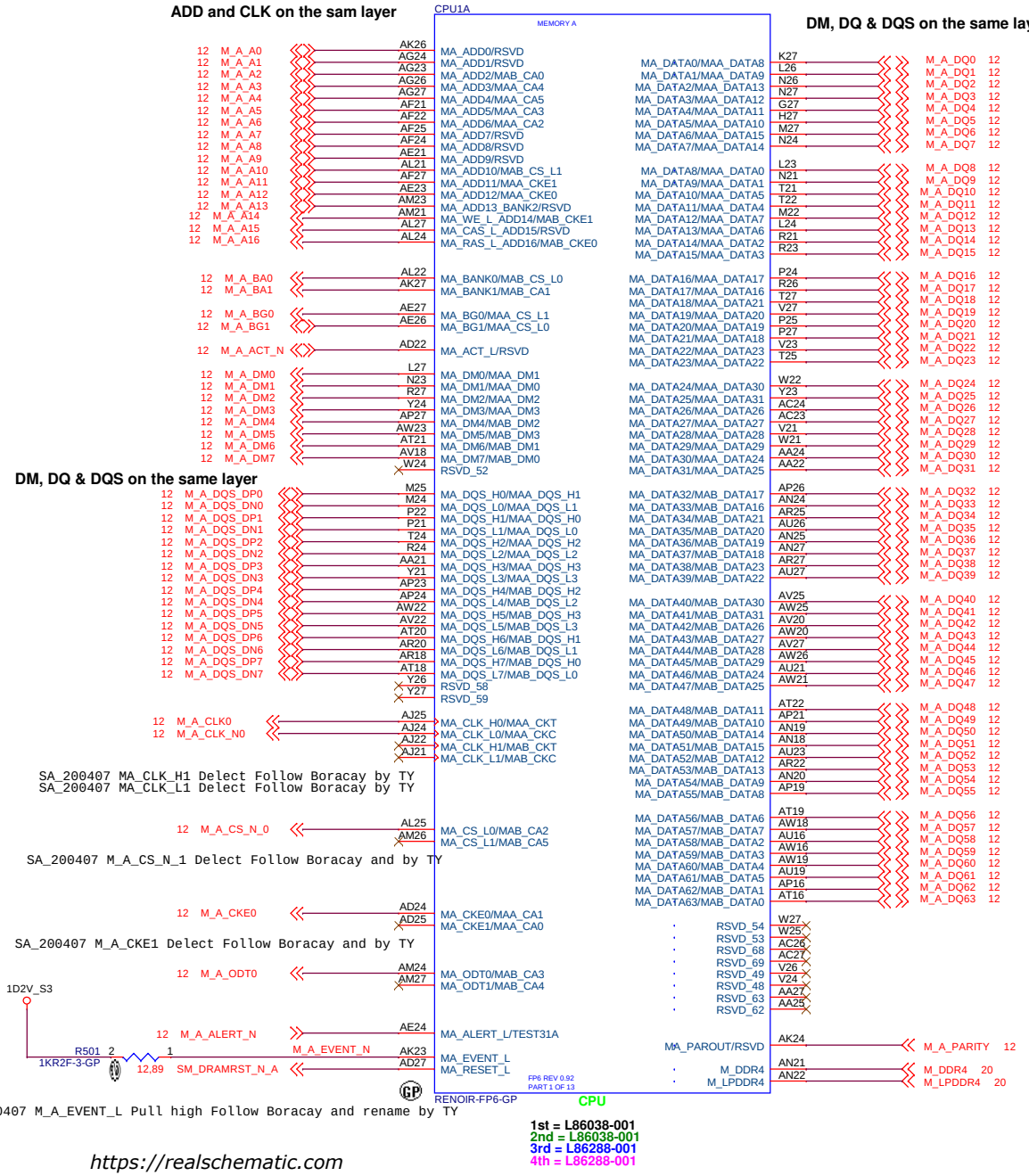
ADD, CMD, CTL, 40Ω
DATA , 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

Layout Note:
DM, DQ & DQS on the same layer
ADD and CLK on the sam layer

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer



1st = L86038-001
2nd = L86038-001
3rd = L86288-001
4th = L86288-001

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A01

緯創資通 Wistron Corporation
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Title: CPU (DDR4_CHA)
Size: A3
Document Number: 13" CS ZURG Lucienne
Rev: -1
Date: Wednesday, March 24, 2021
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Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc.	M_RESET_L	M_EVENT_L	M_ALERT	M_PAROUT

Layout Note:
DM, DQ & DQS on the same layer
ADD and CLK on the sam layer

DDR4
Channel B to DRAM Down

ADD, CMD, CTL, 40Ω
DATA , 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer

CPU1I

MEMORY B

13 M_B_A0	AM29	MB_ADD0/RSVD					
13 M_B_A1	AH31	MB_ADD1/RSVD		MB_DATA0/MBA_DATA8	C27	M_B_DQ0	13
13 M_B_A2	AJ30	MB_ADD2/MBB_CA0		MB_DATA1/MBA_DATA9	A28	M_B_DQ1	13
13 M_B_A3	AH29	MB_ADD3/MBA_CA4		MB_DATA2/MBA_DATA13	F29	M_B_DQ2	13
13 M_B_A4	AG32	MB_ADD4/MBA_CA5		MB_DATA9/MBA_DATA12	F31	M_B_DQ3	13
13 M_B_A5	AG30	MB_ADD5/MBA_CA3		MB_DATA4/MBA_DATA11	B27	M_B_DQ4	13
13 M_B_A6	AG31	MB_ADD6/MBA_CA2		MB_DATA5/MBA_DATA10	D27	M_B_DQ5	13
13 M_B_A7	AF30	MB_ADD7/RSVD		MB_DATA6/MBA_DATA15	E32	M_B_DQ6	13
13 M_B_A8	AG29	MB_ADD8/RSVD		MB_DATA7/MBA_DATA14	F30	M_B_DQ7	13
13 M_B_A9	AF29	MB_ADD9/RSVD					
13 M_B_A10	AM30	MB_ADD10/MBB_CS_L1		MB_DATA8/MBA_DATA0	H31	M_B_DQ8	13
13 M_B_A11	AF31	MB_ADD11/MBA_CKE1		MB_DATA9/MBA_DATA1	H30	M_B_DQ9	13
13 M_B_A12	AE32	MB_ADD12/MBA_CKE0		MB_DATA10/MBA_DATA5	K31	M_B_DQ10	13
13 M_B_A13	AP30	MB_ADD13_BANK2/RSVD		MB_DATA11/MBA_DATA4	L30	M_B_DQ11	13
13 M_B_A14	AP31	MB_WE_L_ADD14/MBB_CKE1		MB_DATA12/MBA_DATA7	G30	M_B_DQ12	13
13 M_B_A15	AP29	MB_CAS_L_ADD15/RSVD		MB_DATA13/MBA_DATA6	H29	M_B_DQ13	13
13 M_B_A16	AN29	MB_RAS_L_ADD16/MBB_CKE0		MB_DATA14/MBA_DATA2	K30	M_B_DQ14	13
				MB_DATA15/MBA_DATA3	K29	M_B_DQ15	13
13 M_B_BA0	AN31	MB_BANK0/MBB_CS_L0		MB_DATA16/MBA_DATA21	N32	M_B_DQ16	13
13 M_B_BA1	AM32	MB_BANK1/MBB_CA1		MB_DATA17/MBA_DATA22	N29	M_B_DQ17	13
				MB_DATA18/MBA_DATA20	P30	M_B_DQ18	13
13 M_B_BG0	AD29	MB_BG0/MBA_CS_L1		MB_DATA19/MBA_DATA19	L32	M_B_DQ19	13
13 M_B_BG1	AD31	MB_BG1/MBA_CS_L0		MB_DATA20/MBA_DATA17	L31	M_B_DQ20	13
				MB_DATA21/MBA_DATA16	M30	M_B_DQ21	13
13 M_B_ACT_N	AD30	MB_ACT_L/RSVD		MB_DATA22/MBA_DATA18	L29	M_B_DQ22	13
				MB_DATA23/MBA_DATA23	N31	M_B_DQ23	13
13 M_B_DM0	C30	MB_DM0/MBA_DM1					
13 M_B_DM1	H32	MB_DM1/MBA_DM0		MB_DATA24/MBA_DATA30	R30	M_B_DQ24	13
13 M_B_DM2	M29	MB_DM2/MBA_DM2		MB_DATA25/MBA_DATA31	R32	M_B_DQ25	13
13 M_B_DM3	T29	MB_DM3/MBA_DM3		MB_DATA26/MBA_DATA26	V30	M_B_DQ26	13
13 M_B_DM4	AU30	MB_DM4/MBB_DM2		MB_DATA27/MBA_DATA27	V32	M_B_DQ27	13
13 M_B_DM5	BD28	MB_DM5/MBB_DM3		MB_DATA28/MBA_DATA28	P29	M_B_DQ28	13
13 M_B_DM6	BB23	MB_DM6/MBB_DM1		MB_DATA29/MBA_DATA29	P31	M_B_DQ29	13
13 M_B_DM7	BD20	MB_DM7/MBB_DM0		MB_DATA30/MBA_DATA25	U31	M_B_DQ30	13
	W31	RSVD_57		MB_DATA31/MBA_DATA24	U29	M_B_DQ31	13
13 M_B_DQS_DP0	E29	MB_DQS_H0/MBA_DQS_H1					
13 M_B_DQS_DN0	D28	MB_DQS_L0/MBA_DQS_L1		MB_DATA32/MBB_DATA16	AT29	M_B_DQ32	13
13 M_B_DQS_DP1	J31	MB_DQS_H1/MBA_DQS_H0		MB_DATA33/MBB_DATA17	AU32	M_B_DQ33	13
13 M_B_DQS_DN1	J29	MB_DQS_L1/MBA_DQS_L0		MB_DATA34/MBB_DATA21	AW31	M_B_DQ34	13
13 M_B_DQS_DP2	N30	MB_DQS_H2/MBA_DQS_H2		MB_DATA35/MBB_DATA20	AW30	M_B_DQ35	13
13 M_B_DQS_DN2	M31	MB_DQS_L2/MBA_DQS_L2		MB_DATA36/MBB_DATA19	AR30	M_B_DQ36	13
13 M_B_DQS_DP3	T30	MB_DQS_H3/MBA_DQS_H3		MB_DATA37/MBB_DATA18	AT31	M_B_DQ37	13
13 M_B_DQS_DN3	T31	MB_DQS_L3/MBA_DQS_L3		MB_DATA38/MBB_DATA23	AV30	M_B_DQ38	13
13 M_B_DQS_DP4	AU29	MB_DQS_H4/MBB_DQS_H2		MB_DATA39/MBB_DATA22	AW29	M_B_DQ39	13
13 M_B_DQS_DN4	AU31	MB_DQS_L4/MBB_DQS_L2					
13 M_B_DQS_DP5	BA27	MB_DQS_H5/MBB_DQS_H3		MB_DATA40/MBB_DATA29	AY29	M_B_DQ40	13
13 M_B_DQS_DN5	BB27	MB_DQS_L5/MBB_DQS_L3		MB_DATA41/MBB_DATA28	AY32	M_B_DQ41	13
13 M_B_DQS_DP6	BC23	MB_DQS_H6/MBB_DQS_H1		MB_DATA42/MBB_DATA24	BC27	M_B_DQ42	13
13 M_B_DQS_DN6	BA23	MB_DQS_L6/MBB_DQS_L1		MB_DATA43/MBB_DATA25	BB26	M_B_DQ43	13
13 M_B_DQS_DP7	BC20	MB_DQS_H7/MBB_DQS_H0		MB_DATA44/MBB_DATA27	BC25	M_B_DQ44	13
13 M_B_DQS_DN7	BA20	MB_DQS_L7/MBB_DQS_L0		MB_DATA45/MBB_DATA26	BA25	M_B_DQ45	13
	Y32	RSVD_61		MB_DATA46/MBB_DATA30	BB30	M_B_DQ46	13
	Y30	RSVD_60		MB_DATA47/MBB_DATA31	BA28	M_B_DQ47	13
13 M_B_CLK0	AJ31	MB_CLK_H0/MBA_CKT					
13 M_B_CLK_N0	AK30	MB_CLK_L0/MBA_CKC		MB_DATA48/MBB_DATA11	BA24	M_B_DQ48	13
	AK32	MB_CLK_H1/MBB_CKT		MB_DATA49/MBB_DATA10	BC24	M_B_DQ49	13
	AL31	MB_CLK_L1/MBB_CKC		MB_DATA50/MBB_DATA14	BC22	M_B_DQ50	13
				MB_DATA51/MBB_DATA15	BA22	M_B_DQ51	13
				MB_DATA52/MBB_DATA12	BB25	M_B_DQ52	13
				MB_DATA53/MBB_DATA13	BD25	M_B_DQ53	13
				MB_DATA54/MBB_DATA9	BB22	M_B_DQ54	13
				MB_DATA55/MBB_DATA8	BD22	M_B_DQ55	13
13 M_B_CS_N_0	AN30	MB_CS_L0/MBB_CA2					
	AR31	MB_CS_L1/MBB_CA5		MB_DATA56/MBB_DATA4	BA21	M_B_DQ56	13
				MB_DATA57/MBB_DATA5	BC21	M_B_DQ57	13
				MB_DATA58/MBB_DATA2	BC18	M_B_DQ58	13
				MB_DATA59/MBB_DATA3	BB18	M_B_DQ59	13
				MB_DATA60/MBB_DATA6	BB20	M_B_DQ60	13
				MB_DATA61/MBB_DATA7	BB21	M_B_DQ61	13
				MB_DATA62/MBB_DATA1	BB19	M_B_DQ62	13
				MB_DATA63/MBB_DATA0	BA18	M_B_DQ63	13
13 M_B_CKE0	AC31	MB_CKE0/MBA_CA1					
	AC29	MB_CKE1/MBA_CA0		RSVD_56	W30		
				RSVD_55	W29		
				RSVD_65	AA30		
				RSVD_67	AB29		
13 M_B_ODT0	AP32	MB_ODT0/MBB_CA3		RSVD_50	V29		
	AR29	MB_ODT1/MBB_CA4		RSVD_51	V31		
				RSVD_64	AA29		
				RSVD_66	AA31		
13 M_B_ALERT_N	AE30	MB_ALERT_L/TEST31B					
M_B_EVENT_L	AL30	MB_EVENT_L		MB_PAROUT/RSVD	AM31	M_B_PARITY	13
13,89 SM_DRAMRST_N_B	AC32	MB_RESET_L					

FP6 REV 0.92
PART 9 OF 13

RENOIR-FP6-GP

CPU

1D2V_S3

R601 2 1 1KR2F-3-GP

SA_200407 MB_CLK_H1 Delect Follow Boracay by TY
SA_200407 MB_CLK_L1 Delect Follow Boracay by TY

SA_200407 M_B_CS_N_1 Delect Follow Boracay and by TY

SA_200407 M_B_CKE1 Delect Follow Boracay and by TY

SA_200407 MB_ODT1 Delect Follow Boracay by TY

SA_200406 M_B_EVENT_L Pull high Follow Boracay and rename by TY

1st = L86038-001
2nd = L86038-001
3rd = L86288-001
4th = L86288-001

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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR4_CHB)

Size: A3 | Document Number: 13" CS ZURG Lucienne | Rev: -1

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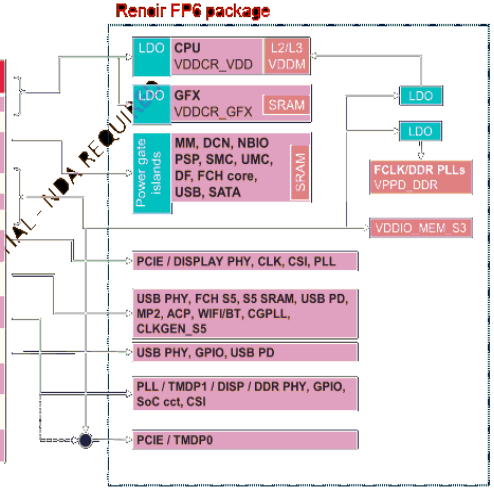
Table 7. FP6 Processor Voltage Supply Currents for AMD Family 17h Models 60h-6Fh Processors

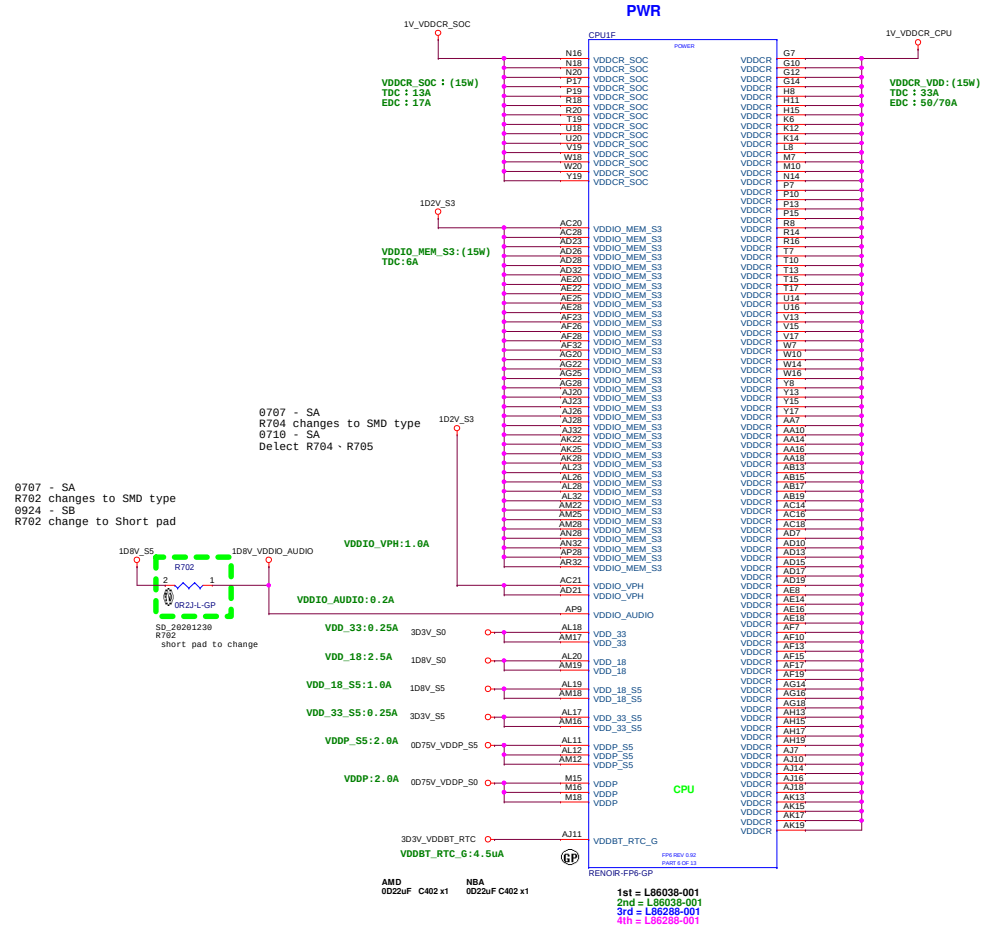
NOTICE: To identify the proper requirements for AMD Family 17h Models 60h and AMD Family 17 Models 68h, see notes 8 and 9.								
Supply [1]	**Nominal Voltage at Pkg Ball (V) [2]**	**Condition**	**SYSTEM_CONFIGURATION**					
			1 10 W	**2 15 W**	**3 25 W**	**4 35 W**	**5 45 W**	**6 54 W**
VDDCR_VDD	Variable	TDC [3]	20	33	44	51	58	
		EDC	34	50[8]/70[9]	70	90	96	
	(0.6-1.55) [5]	Max Loadstep [4]	29	43[8]/65[9]	65	76	84	
VDDCR_SOC	Variable	TDC [3]	10	13		15		
		EDC	13	17		20		
	(0.6-1.55) [5]	Max Loadstep [4]	10	13		15		
VDDIO_MEM_S3 [6]	1.10	TDC	6.00					
	1.20	TDC	6.00					
VDDIO_VPH [7]	1.20	TDC	1.00					
	1.80	TDC	1.00					
VDDP	0.75	TDC	2.00					
VDDP_S5	0.75	TDC	2.00					
VDD_18	1.80	TDC	2.50					
VDD_18_S5	1.80	TDC	1.00					
VDD_33	3.30	TDC	0.25					
VDD_33_S5	3.30	TDC	0.25					
VDDIO_AUDIO	1.20	TDC	0.20					
	1.50	TDC	0.20					
	1.80	TDC	0.20					
VDDBT_RTC_G	3.00	TDC	4.5 µA					

#56178 v1.03

VDDIO_VPH	VDDIO_VPH is a dedicated power supply for DisplayPort 0. When • DP0 is used for eDP, connect VDDIO_VPH to VDDIO_MEM_S3 source (1.2V DDR4) or other 1.2V source to improve battery life. Or connect to VDD_18 source (1.8V) if no 1.2V source is available. • DP0 is used for DP or HDMI, connect VDDIO_VPH to VDD_18 source (1.8V).

FP6 PACKAGE RAIL	SoC IP RAIL	S0i2	S0i3	S3
VDDCR (0.65 – 1.3V, 65A)	VDDCR_VDD	Off	Off	Off
	VDDCR_GFX	Off	Off	Off
VDDCR_SOC (0.675 – 1.05V, 10A)	VDDCR_SOC	Low	Off	Off
VDDIO_MEM_S3 (1.1/1.2V, 7A)	VDDIO_MEM_S3	ON	ON	ON
	VDDM	Off	Off	Off
	VDDP_DDR	Off	Off	Off
VDDP (0.75V, 2A)	VDDP	ON	Off	Off
VDDP_S5 (0.75V, 2A)	VDDP_S5	ON	ON	ON
VDD_18 (1.8V, 2.5A)	VDD_18	ON	Off	Off
VDD_18_S5 (1.8V, 0.5A)	VDD_18_5	ON	ON	ON
VDD_33 (3.3V, 0.25A)	VDD_33	ON	Off	Off
VDD_33_S5 (3.3V, 0.25A)	VDD_33_S5	ON	ON	ON
VDD_AUD_S5 (1.8V, 0.25A)	VDD_AUD_S5	ON	ON	ON





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DISPLAY/SVI/JTAG/TEST

DisplayPort	Device
0	eDP
1	HDMI
2	DP
3	

PINOUT	Description
DP_BLON	BL_ENABLE
DP_DIGON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

HDT PIN Pull High Resistor
ASM if HDT CONN is needs of use

0702 -SA
SIC/SID change to pull high to 1.8V_S0

0707 - SA
R816~R820 change to SMD type
0924 - SB
R816~R820 change to short pad

PU FOR AMD INTERNAL
PD FOR CUSTOMER

Figure 136. Routing Diagram for Voltage Sense Signals

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Title: CPU (DP/SVI/JTAG/TEST)

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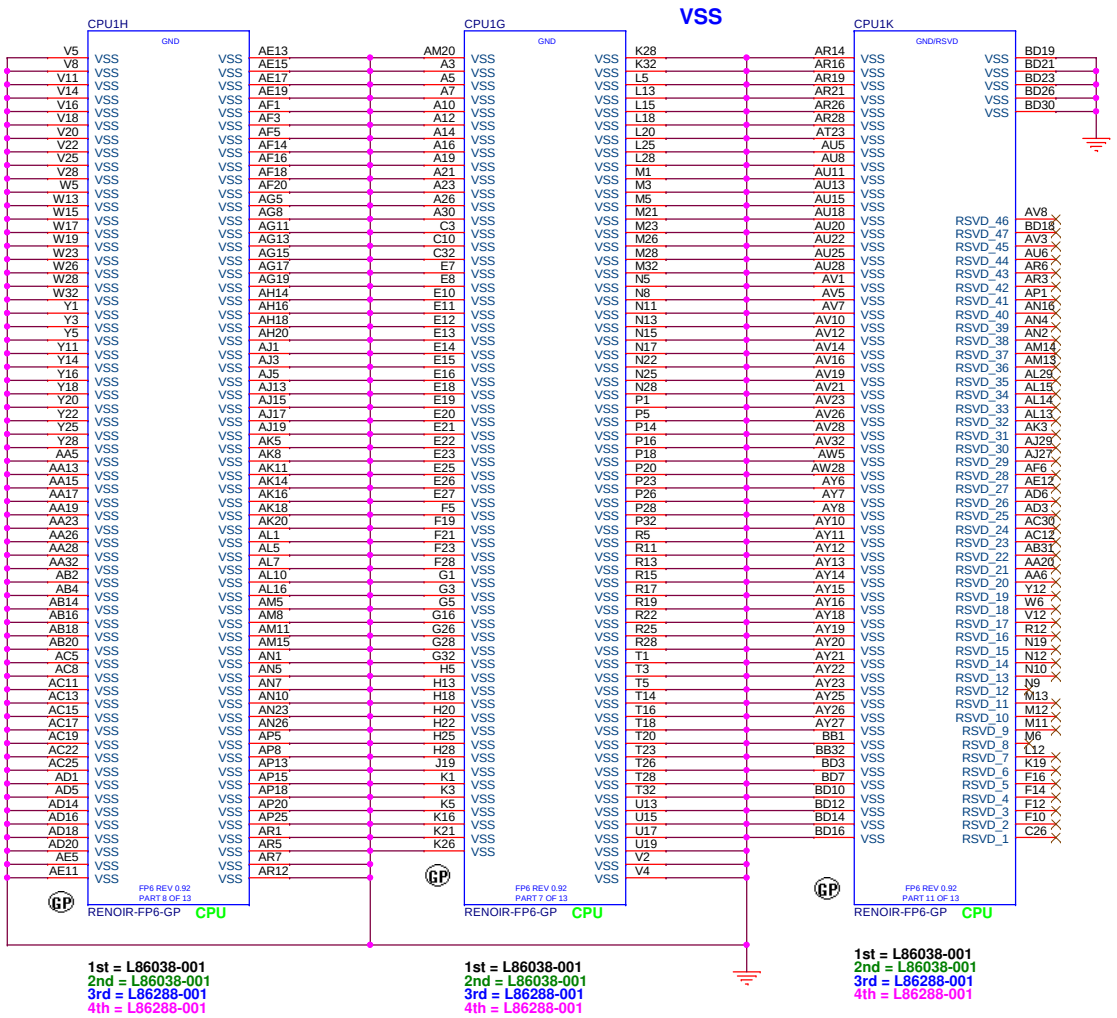

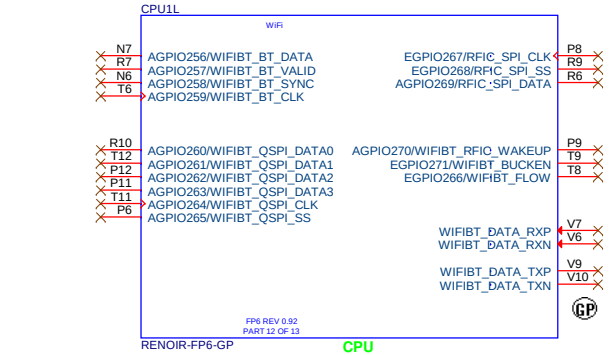

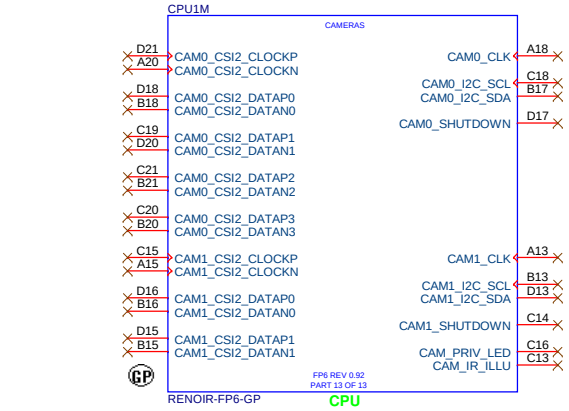

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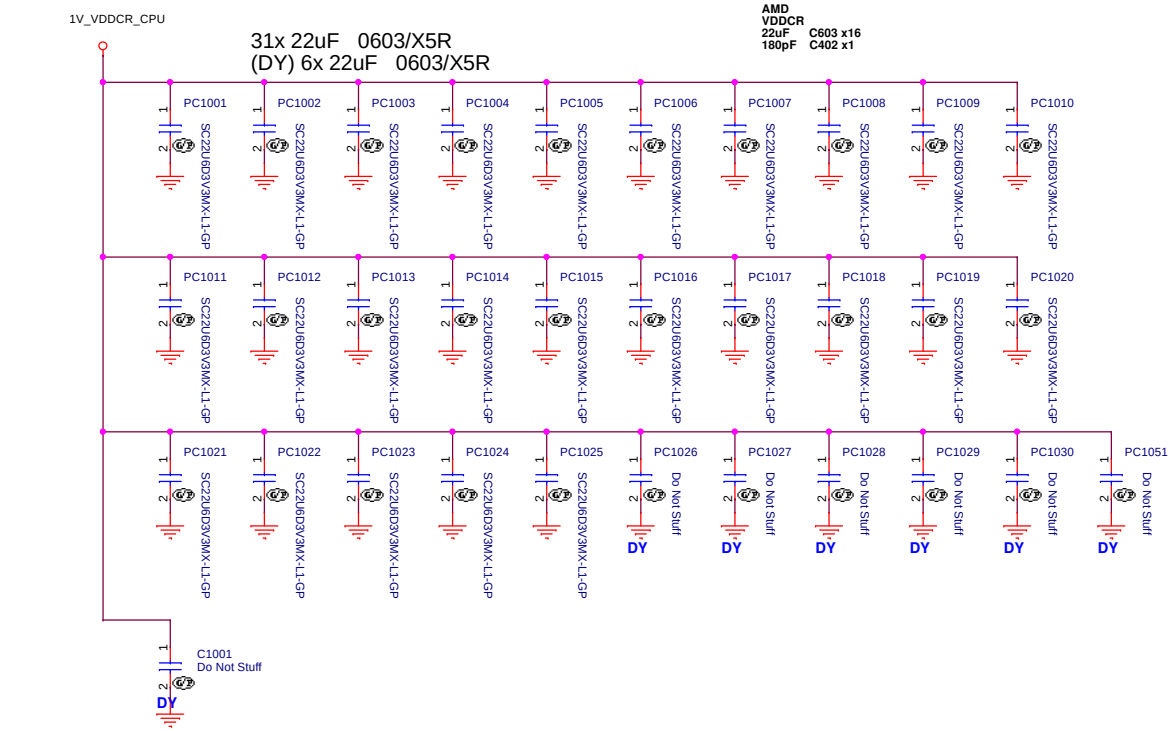
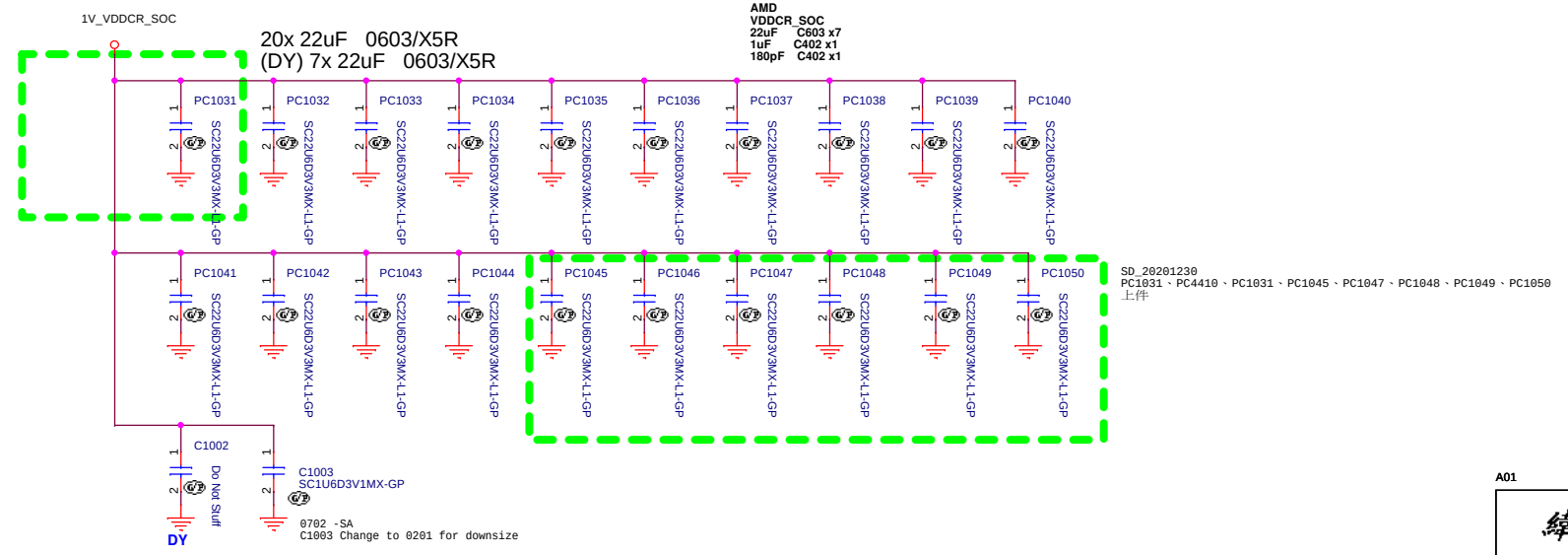
APU Caps





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Title: ***CPU (POWER CAP1)***

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APU Caps

AMD
VDDIO_MEM_S3
22uF C603 x9
1uF C402 x2
0D22uF C402 x4
180pF C402 x1

1D2V_S3

C1101 SC22U6D3V3MX-L1-GP
C1102 SC22U6D3V3MX-L1-GP
C1103 SC22U6D3V3MX-L1-GP
C1104 SC22U6D3V3MX-L1-GP
C1105 SC22U6D3V3MX-L1-GP
C1106 SC22U6D3V3MX-L1-GP
C1107 SC22U6D3V3MX-L1-GP
C1153 SC22U6D3V3MX-L1-GP
C1154 SC22U6D3V3MX-L1-GP

C1108 SCD22U10V2KX-L1-GP
C1109 SCD22U10V2KX-L1-GP
C1110 SCD22U10V2KX-L1-GP
C1111 SCD22U10V2KX-L1-GP

C1114 SC1U6D3V1MX-GP
C1115 SC1U6D3V1MX-GP
C1116 Do Not Stuff
DY

0702 -SA
C1114 Change to 0201 for downsize
C1115 Change to 0201 for downsize

AMD
VDDP_S5
22uF C603 x1
1uF C402 x3

0D75V_VDDP_S5

C1118 SC22U6D3V3MX-L1-GP
C1119 SC1U6D3V1MX-GP
C1120 SC1U6D3V1MX-GP
C1121 SC1U6D3V1MX-GP

0702 -SA
C1119 Change to 0201 for downsize
C1120 Change to 0201 for downsize
C1121 Change to 0201 for downsize

AMD
VDDP_S0
22uF C603 x1
1uF C402 x8
180pF C402 x1

0D75V_VDDP_S0

C1142 SC22U6D3V3MX-L1-GP
C1117 Do Not Stuff
DY
C1155 SC22U6D3V3MX-L1-GP

C1143 SC1U6D3V1MX-GP
C1144 SC1U6D3V1MX-GP
C1145 SC1U6D3V1MX-GP
C1146 SC1U6D3V1MX-GP
C1147 SC1U6D3V1MX-GP

0702 -SA
C1143~50 Change to 0201 for downsize

C1148 SC1U6D3V1MX-GP
C1149 SC1U6D3V1MX-GP
C1150 SC1U6D3V1MX-GP

AMD
VDD_33_S5
22uF C603 x1
1uF C402 x2

3D3V_S5

C1130 SC22U6D3V3MX-L1-GP
C1131 SC1U6D3V1MX-GP
C1132 SC1U6D3V1MX-GP

0702 -SA
C1131 Change to 0201 for downsize
C1132 Change to 0201 for downsize

AMD
VDD_33
22uF C603 x1
1uF C402 x2

3D3V_S0

C1135 SC22U6D3V3MX-L1-GP
C1136 SC1U6D3V1MX-GP
C1137 SC1U6D3V1MX-GP

0702 -SA
C1136 Change to 0201 for downsize
C1137 Change to 0201 for downsize

AMD
VDDBT_RTC_G
1uF C402 x1
0D22uF C402 x1

3D3V_VDDBT_RTC

C1140 SC1U6D3V1MX-GP
C1141 SCD22U10V2KX-L1-GP

0702 -SA
C1140 Change to 0201 for downsize

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Table 132. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S3[1, 2]	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 µF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 µF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 µF	0402 X5R	-	-	4 along split	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2 along split	1BU	-	-	-	-	-	-	-

Key: *Capacitor locations are marked as follows: BU = Bottom, Under the processor, BO = Bottom, Outside of the processor, T = Top, same side as the Processor S = Close to VDDIO_MEM_S3 plane split*

AMD
VDD_18_S5
22uF C603 x1
1uF C402 x2

1D8V_S5

C1122 SC22U6D3V3MX-L1-GP
C1123 SC1U6D3V1MX-GP
C1124 SC1U6D3V1MX-GP

0702 -SA
C1123 Change to 0201 for downsize
C1124 Change to 0201 for downsize

AMD
VDDIO_AUDIO
22uF C603 x1
1uF C402 x1

1D8V_VDDIO_AUDIO

C1128 SC22U6D3V3MX-L1-GP
C1129 SC1U6D3V1MX-GP

0702 -SA
C1129 Change to 0201 for downsize

AMD
VDD_18
22uF C603 x1
1uF C402 x2

1D8V_S0

C1125 SC22U6D3V3MX-L1-GP
C1126 SC1U6D3V1MX-GP
C1127 SC1U6D3V1MX-GP

0702 -SA
C1126 Change to 0201 for downsize
C1127 Change to 0201 for downsize

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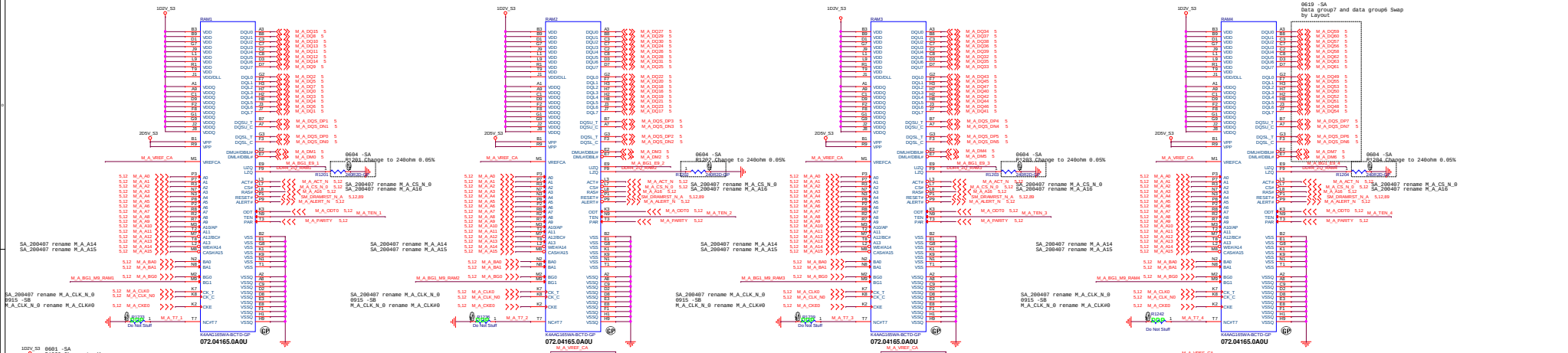
Main Func = DDR4 DRAM Down



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Title	DDR (DDR4-CHA)
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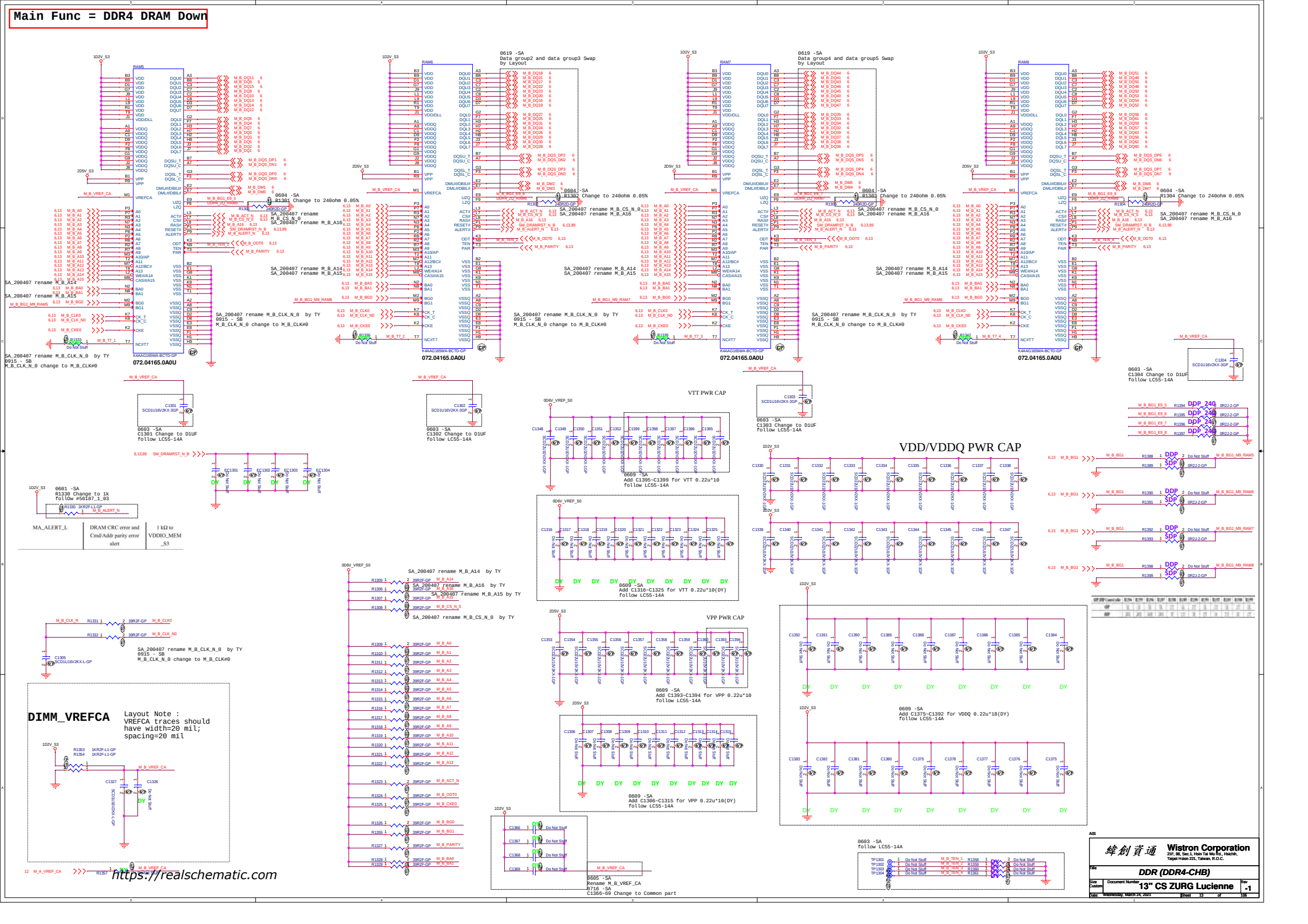
Main Func = DDR4 DRAM Down



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Title
DDR (RSVD)

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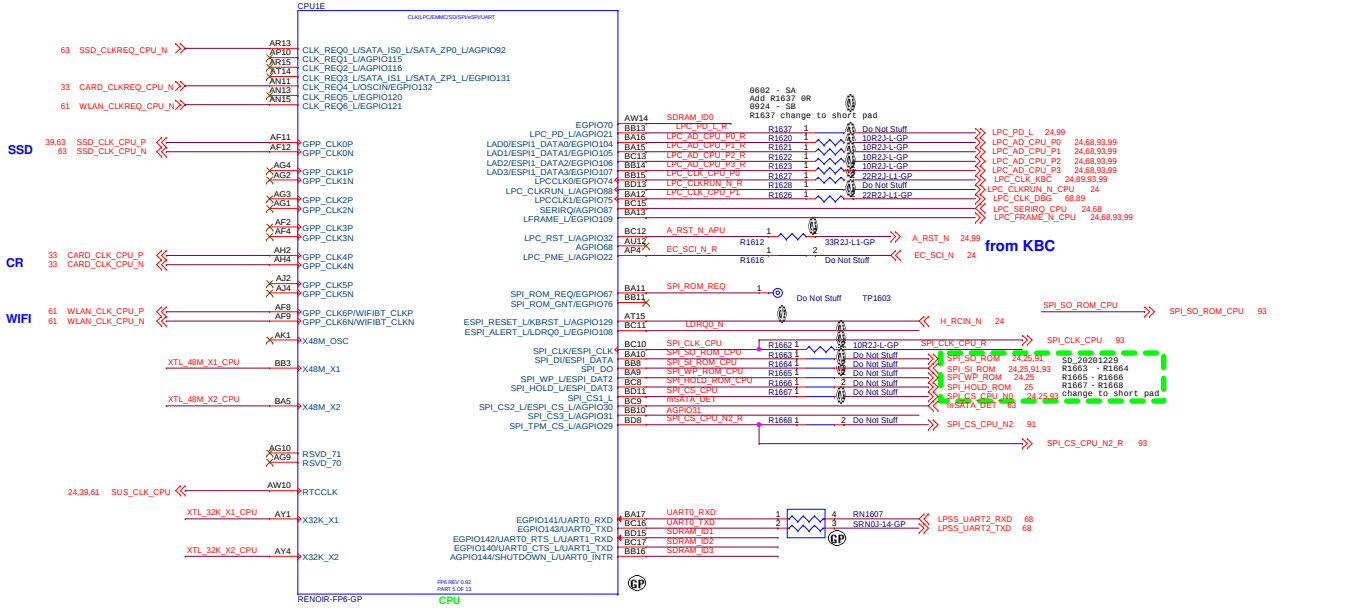
CLK/SATA/USB/SPI/LPC

P_GFX port	Device	CLK port	CLKREQ#
0	N/A	N/A	N/A
1	N/A	N/A	N/A
2	N/A	N/A	N/A
3	N/A	N/A	N/A
4	N/A	N/A	N/A
5	N/A	N/A	N/A
6	N/A	N/A	N/A
7	N/A	N/A	N/A

P_GPP port	Device	CLK port	CLKREQ#
0	M.2 SSD		
1	M.2 SSD	0	0
2	M.2 SSD		
3	M.2 SSD		
4	CR	4	4
5	N/A	N/A	N/A
6	N/A	N/A	N/A
7	WIFI	6	6
8	N/A	N/A	N/A
9	N/A	N/A	N/A
10	N/A	N/A	N/A
11	N/A	N/A	N/A

LPCCLK1/EGPIO75
CLK_REQ5_L
If unused,
enable internal pull up or pull down by software.

GFX & GPP CLK, 85Ω
SATA & USB, 90Ω



	Vendor	Part number	model	SDP/DDP	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Size	DB	SI	SI-2	PV
Drop	Hynix (TG)	L31665-381	H5ANAG6NCMR-XNC	DDP	0	0	0	0	16Gb	SKU3			
	Micron (TF)	L31665-682	MT40A1G16KD-062E:E	SDP	0	0	0	1	16Gb	SKU5		SKU6	SKU4
	Samsung (TH)	L31665-981	K4AAG165WA-BCWE	SDP	0	0	1	0	16Gb	SKU6	SKU4	SKU4	SKU2
	Hynix (TG)	L31664-372	H5AN8G6NDJR-XNC	SDP	0	0	1	1	8Gb	SKU1	SKU1	SKU1	
	Micron (TF)	L31664-672	MT40A512M16TB-062E:J	SDP	0	1	0	0	8Gb	SKU4	SKU3	SKU3	
	Samsung (TH)	L31664-971	K4A8G165WC-BCWE	SDP	1	0	0	0	8Gb	SKU2		SKU5	SKU1
SI add	Hynix (TG)	L31665-382	H5ANAG6NCJR-XNC	SDP	1	0	0	1	16Gb		SKU2	SKU2	SKU3

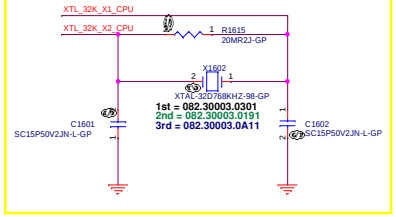
SD_20201229
PAV 13 CS_Zurg_CZN PV IUR plan_v0.5_1223

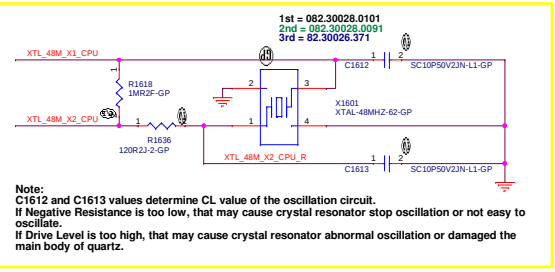
0914 - SB
Remove C1603 for common part

0729 - SA
X1601 add 3rd source 82.30026.371
0917 -SB
X1601 change 2nd to 082.30028.0091
by Soucer
C1612=C1613=10PF(78.10034.L0L)
R1636=120R
by XTAL report (3crystal vendor)

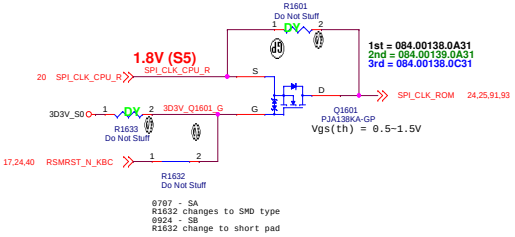
1st: 082.30003.0301 - SEIKO
2nd: 082.30003.0191 - EPSON
3rd: 082.30003.0A11 - TAITIEN

0729 - SA
X1602 add 3rd source 82.30003.0A11





Note:
C1612 and C1613 values determine CL value of the oscillation circuit.
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.



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Title	CPU (CLK/LPC/SPI/EMMC/SD/UART)
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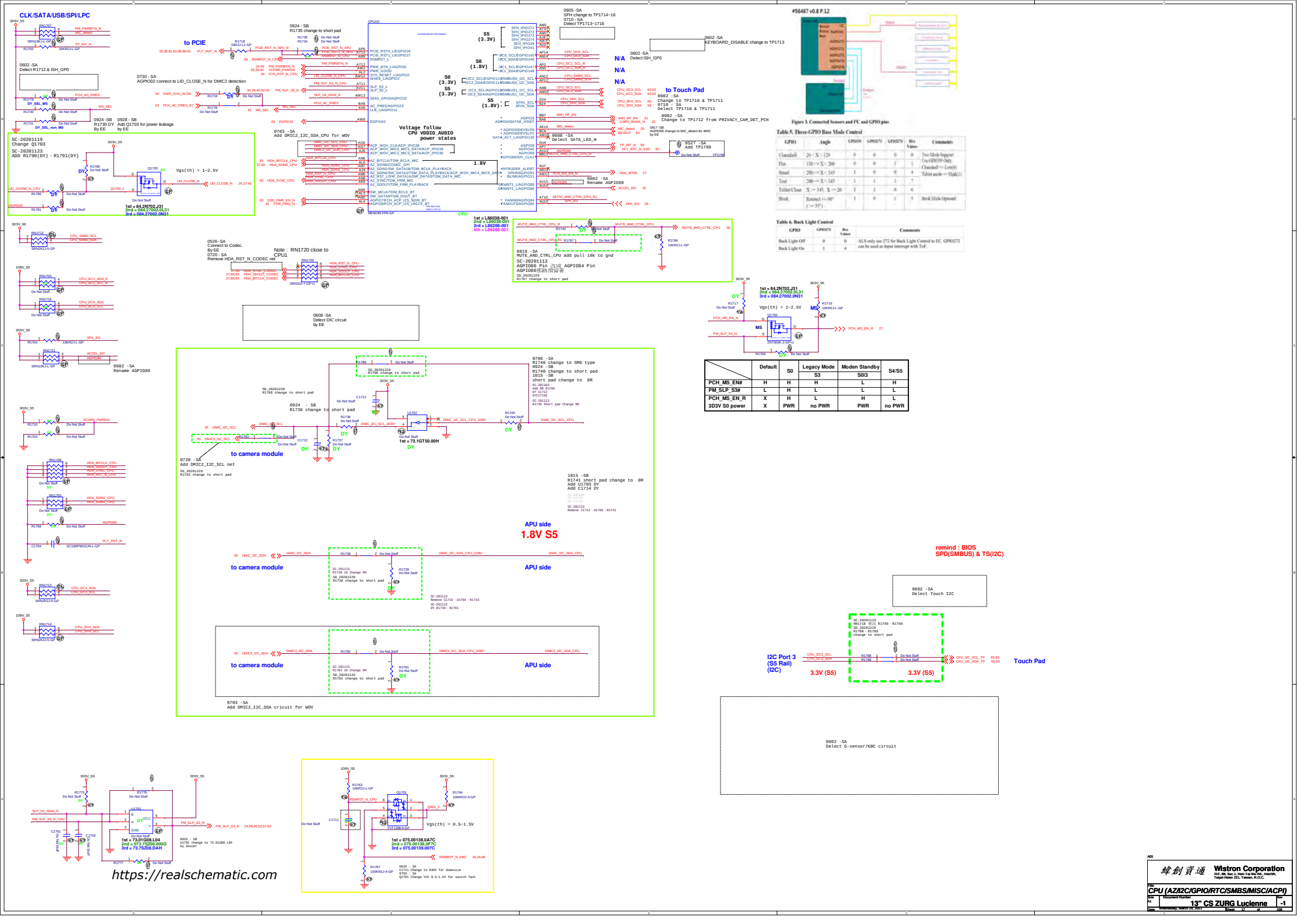
CLK/SATA/USB/SPI/LPC
to PCIE
to Touch Pad
Voltage follow
CPU VDDIO_AUDIO
power states
to camera module
APU side
1.8V S5
remind : BIOS
SPD(SMBUS) & TS(I2C)
I2C Port 3
(S5 Rail)
(I2C)
3.3V (S5)
Touch Pad
CPU (AZ/I2C/GPIO/RTC/SMBS/MISC/ACPI)
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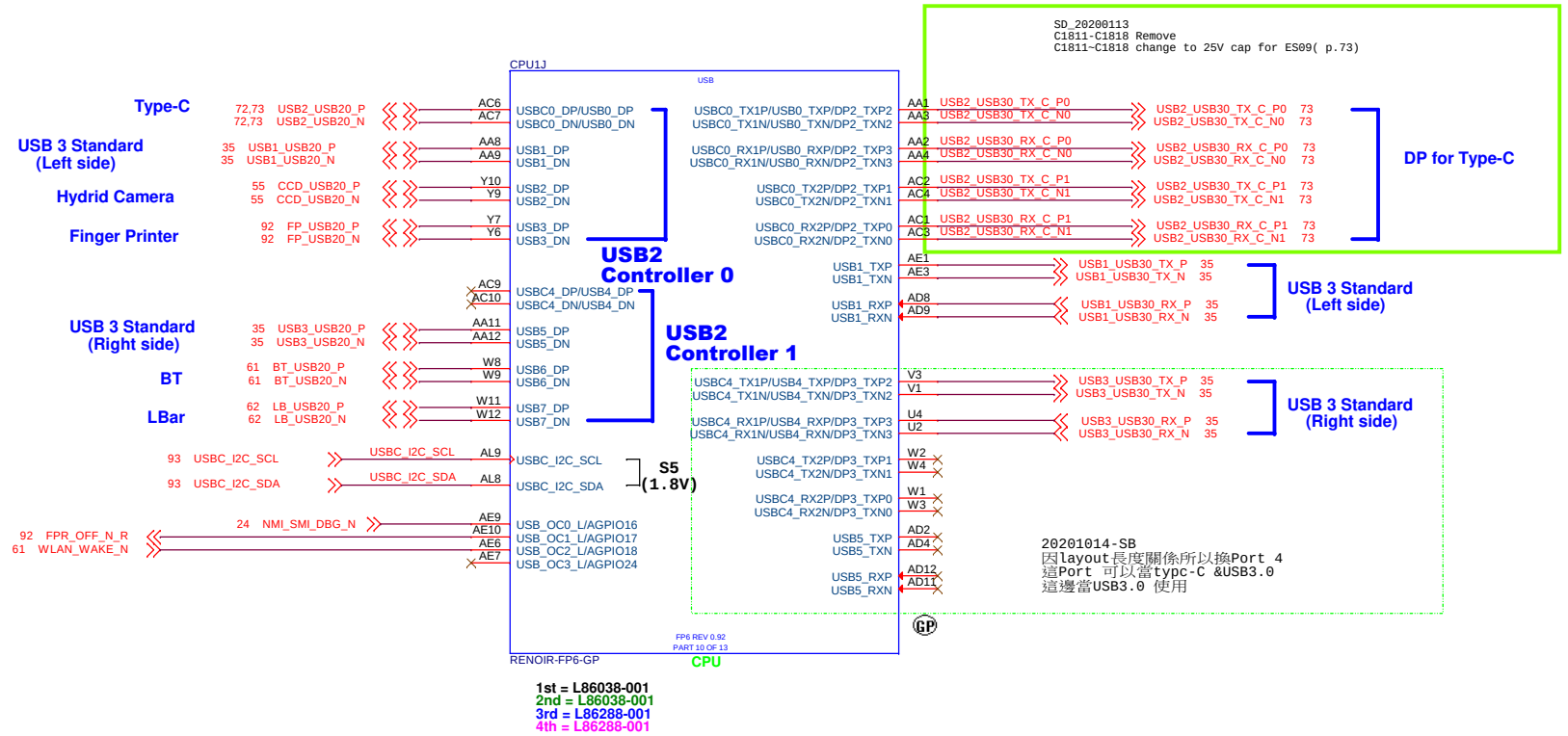

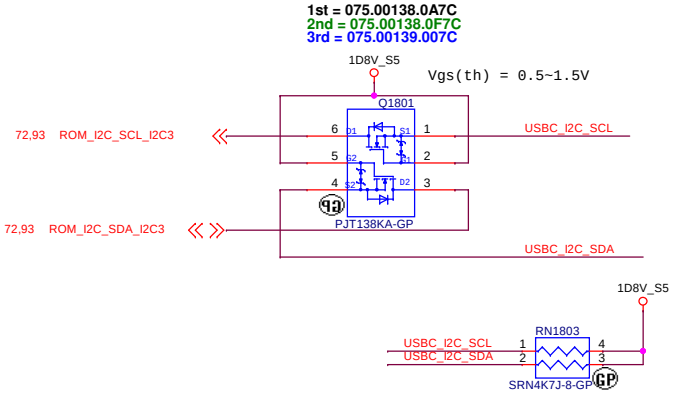

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Size: A3 | Document Number: 13" CS ZURG Lucienne | Rev: -1

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Title: CPU (RSVD)

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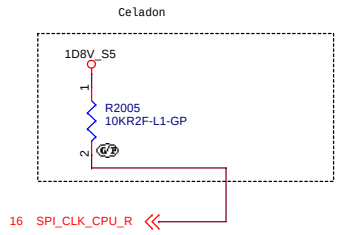
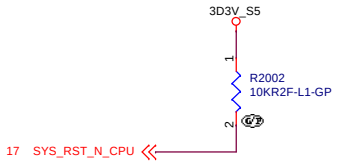
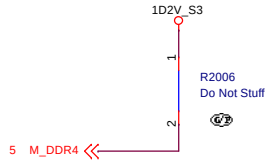
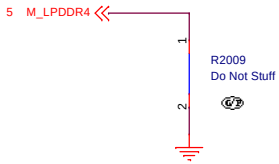
STRAP PINS

GPIO	SPI _ CLK/ESPI_CLK	SYS_RESET_L/AGPIO1
Schematic		
GPIO	**M_DDR4**	**M_LPDDR4**
Schematic		

#56179 v0.81
If unused,
enable internal pull up or pull down by software.

CLK	CLK_REQ5_L/EGPIO120
Misc	PCIE_RST0_L/EGPIO26
GPIO	AGPIO40
SMBus	I2C0_SCL/EGPIO145 I2C0_SDA/EGPIO146 I2C1_SCL/EGPIO147 I2C1_SDA/EGPIO148 I2C2_SCL/EGPIO113/SMBUS0_I2C_SCL I2C2_SDA/EGPIO114/SMBUS0_I2C_SDA I2C3_SCL/AGPIO19/SMBUS1_I2C_SCL I2C3_SDA/AGPIO20/SMBUS1_I2C_SDA
LPC	LPC_PD_L/AGPIO21 LPC_RST_L/AGPIO32 LFRAME_L/EGPIO109 LPCCLK0/EGPIO74 LPCCLK1/EGPIO75
ACPI	LLB_L/AGPIO12
SPI	SPI_TPM_CS_L/AGPIO29

#56178 v0.81 P.231

STRAP PINS

PIN NET	SPI_CLK (SPI_CLK_ROM)	SYS_RESET_L//AGPIO1 (SYS_RST#_CPU)	M_DDR4	M_LDDR4
PULL HIGH	Configured for internal clock-generator 10kΩ (± 5%) pull-up resistor to VDD_18_S5 (DEFAULT)	Normal powerup / reset timing 10KΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)	Enable DDR4 memory controller 0ohm (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3 (DEFAULT)	Enable LPDDR4x memory controller 0ohm (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3
PULL LOW	Reserved	Reserved	Disable DDR4 (need to have LPDDR4x enabled) 0ohm (± 5%) pull-down resistor or direct connect to VSS	Disable LPDDR4x (need to have DDR4 enabled) 0ohm (± 5%) pull-down resistor or direct connect to VSS (DEFAULT)

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Strappings)

Size: A3 | Document Number: 13" CS ZURG Lucienne | Rev: -1

Date: Wednesday, March 24, 2021 | Sheet 20 of 106

TBD

A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*FCH (RSVD)*	
Size A3	Document Number **13" CS ZURG Lucienne**	Rev **-1**
Date: Wednesday, March 24, 2021	Sheet 21 of 106	

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TBD

A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *FCH (RSVD)*

Size	Document Number	Rev
A3	13" CS ZURG Lucienne	-1

Date: Wednesday, March 24, 2021 Sheet 22 of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *FCH (RSVD)*

Size	Document Number	Rev
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https://realschematic.com

SSID = KBC

HP Limit Signal Detect

PCB VERSION

PCB_VERSION	Full Low Register	Full High Register	Typical Voltage	Max Voltage	X32C Firmware Setting	
5A	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
5B	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
5C	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
5D	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
5E	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
-1	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
-2	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
-1 low power hibernation	100.0 K	148.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
5C low power hibernation	100.0 K	174.0 K	1.264 V	1.320 V	>= 1.126 V	< 1.281 V
5B low power hibernation	100.0 K	215.0 K	1.048 V	1.062 V	>= 1.062 V	< 1.126 V

MODEL ID

MODEL_ID_A0	Full Low Register	Full High Register	Typical Voltage	Max Voltage	KBC Firmware Setting		EC ID A31 Val?
13"Zurg AMD Lucienne UMA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V		0x60
13"Zurg AMD Cezanne UMA	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V	0x61

	RID	X9	X2	ADT_TYPE_A.D(V)
	v	k ohm	k ohm	
45w	19.5	499	0.1	0.2	0.2190
65w	19.5	383	0.1	0.2	0.4130
90w	19.5	294	0.1	0.2	0.5354
120w	19.5	221	0.1	0.2	0.7058
135w	19.5	169	0.1	0.2	0.9129
150w	19.5	130	0.1	0.2	1.1702
180w	19.5	100	0.1	0.2	1.4945
200w	19.5	95.257	0.1	0.2	1.7306
230w	19.5	72.752	0.1	0.2	1.8968
260W	19.5	64.9	0.1	0.2	2.2011
280W	19.5	57.6	0.1	0.2	2.4560
330w	19.5	42.2	0.1	0.2	3.0280

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Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ECIO(NPCE38APB0DX)
Size	A1
Document Number	13" CS ZURG Lucienne
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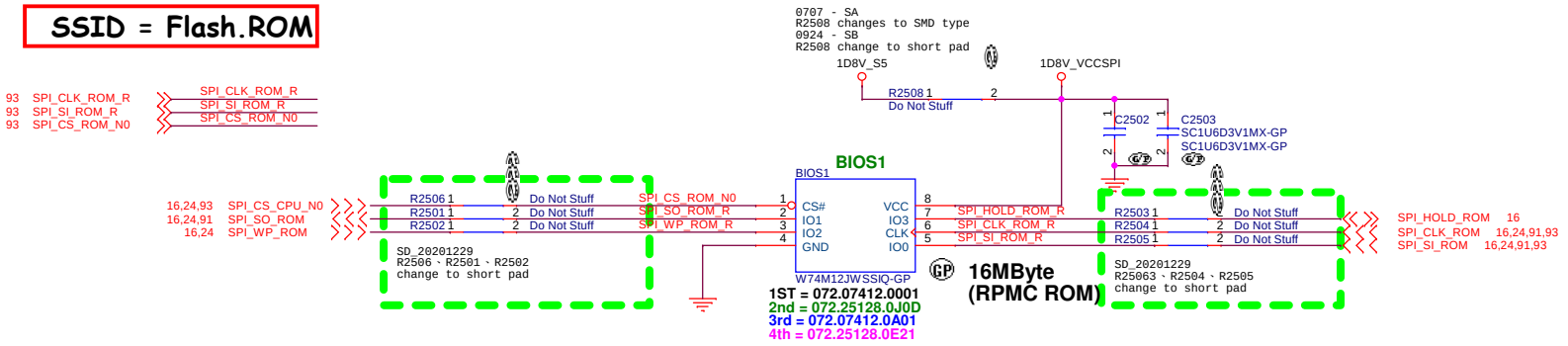
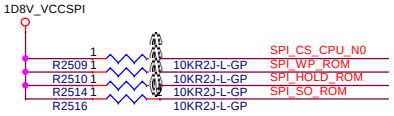
SSID = Flash.ROM



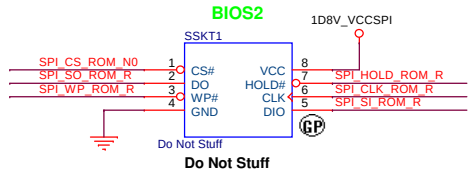


廠商	容量	包裝	廠商料號	緯創料號	備註	RPMC	DB	SI	PV
Gigadevice	128	WSON8(6*5)	GD25LR128DWIGR	072.25128.0E21	QE=1;1.8V	YES		SKU4	
	128	SOP8	GD25LR128DSIGR	072.25128.0J0D	QE=1;1.8V	YES		SKU2	
Winbond	128	WSON8(6*5)	W74M12JWZPIQ	072.07412.0A01	QE=1;1.8V	YES	SKU1	SKU3	
	128	SOP8	W74M12JWSSIQ	072.07412.0001	QE=1;1.8V	YES		SKU1	
XMC	128	WSON8(6*5)	XM25RU128CWIQT08H	072.25128.0AH1	QE=1;1.8V	YES			
	128	SOP8	XM25RU128CHIQT08H	072.25128.0AG1	QE=1;1.8V	YES			

XMC-->AVL(X)不使用

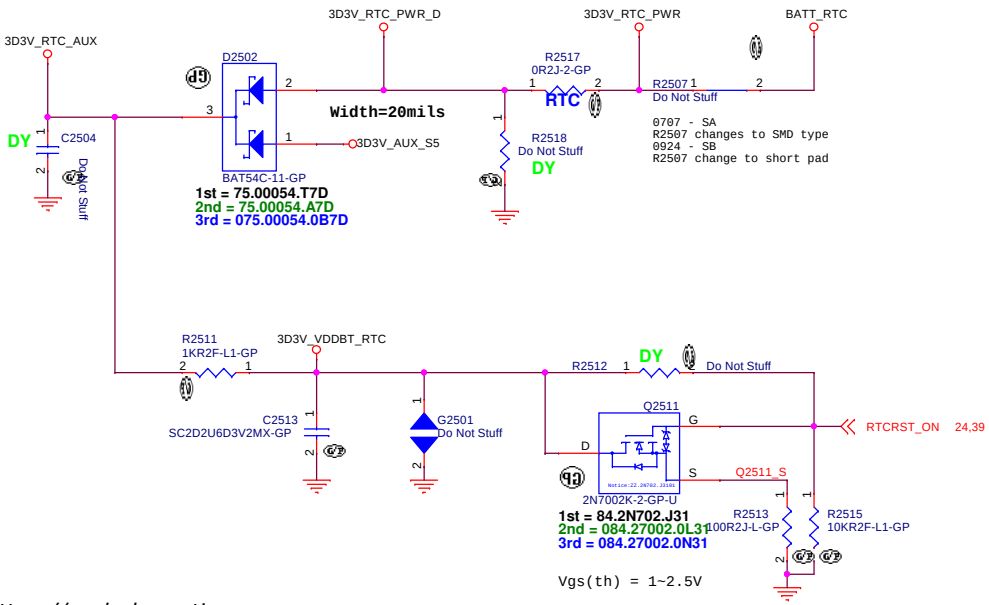
SPI Scoket (WSON)

Co-lay with BIOS1
Socket (62.10076.031) (SOP8)
Socket (062.10029.0131) (WSON)(6*5)



1st = 62.10076.031
2nd = 62.10076.031
3rd = 062.10029.0131
4th = 062.10029.0131

SSID = RBAT



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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: A3
Document Number: 13" CS ZURG Lucienne
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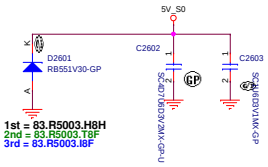
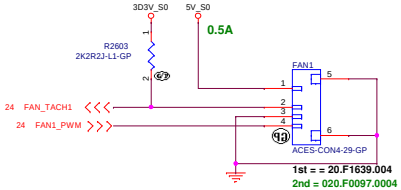
SSID = Thermal

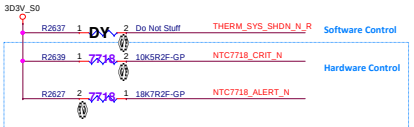
Layout 15 mil



0603 - SA
Delect FAN2
by EE



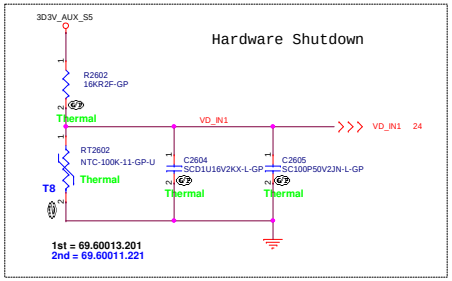
0603 -SA
FAN1 change for emn
0821 -SA
FAN1_swap pin define
by EE
0903 -SB
add 2nd 020.F0097.0004



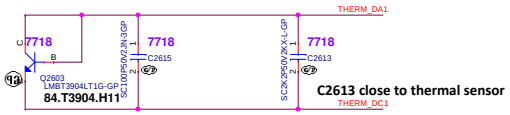
R2627 \ R2639	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

1.1 Product Selection Guide

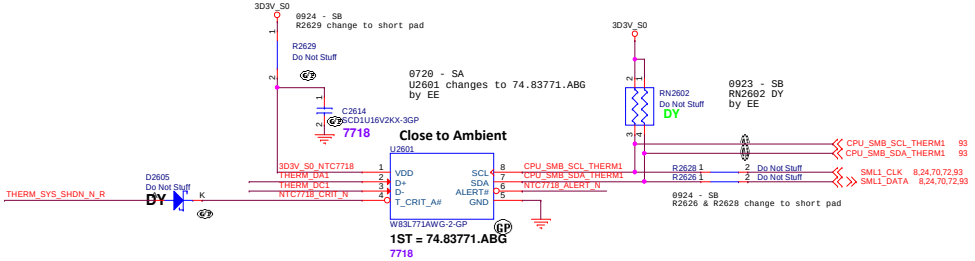
PART NUMBER	SMBUS ADDRESS	FUNCTIONALITY			PACKAGE
		REMOTE	LOCAL	OTHER	
W83L771AWG	1001_100xb				TSSOP-8
W83L771AWG-2	1001_101xb			Programmable temperature High/Low limit	(MSOP-8)
W83L771ASG	1001_100xb				SOP-8
W83L771ASG-2	1001_101xb				

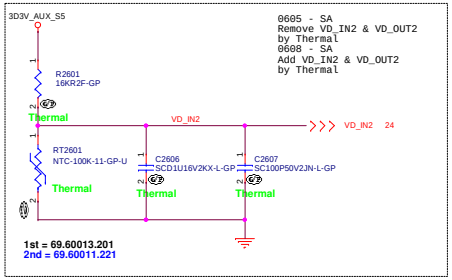


0519 - SA
Add VD_IN1 circuit
by EE



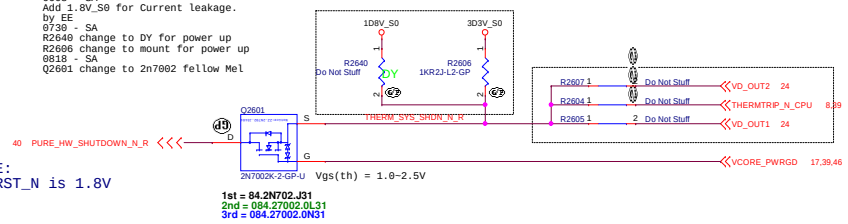
Close to CPU





0605 - SA
Remove VD_IN2 & VD_OUT2
by Thermal
0608 - SA
Add VD_IN2 & VD_OUT2
by Thermal

0608 - SA
Add 1.8V_S0 for Current leakage.
by EE
0730 - SA
R2640 change to DY for power up
R2606 change to mount for power up
0818 - SA
Q2601 change to 2n7002 fellow Mel



NOTE:
ECRST_N is 1.8V

0519 - SA
Add VD_OUT2 NET
by EE
0605 - SA
Delect VD_OUT2 NET
by Thermal
0608 - SA
Add VD_OUT2 NET
by Thermal
0707 - SA
R2604、R2605、R2607 change to SMD type
0924 - SB
R2604、R2605、R2607 change to short pad

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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Thermal/Fan)

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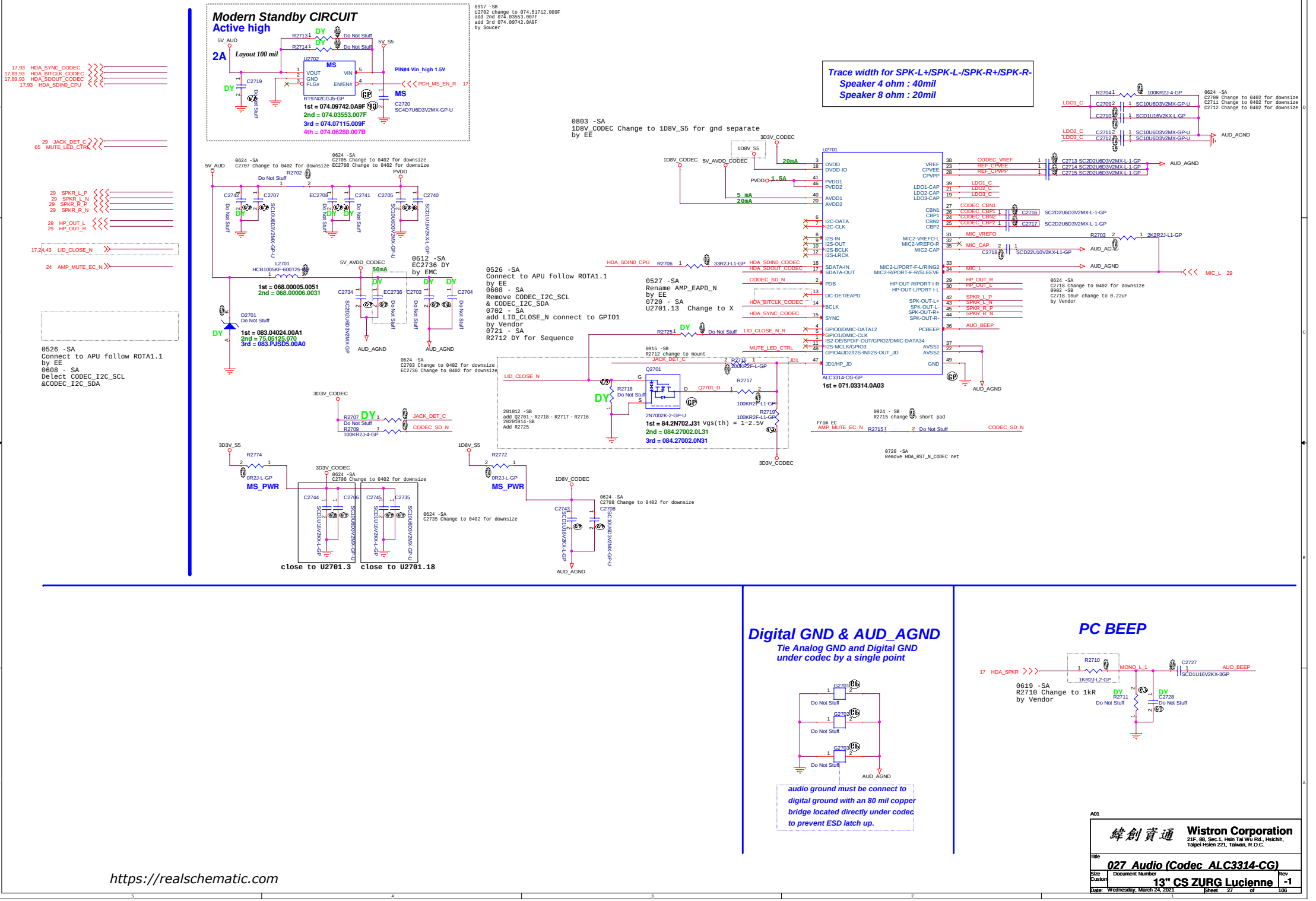
Modern Standby CIRCUIT
Active high
2A
Layout 100 mil
5V_AUD
5V_S5
U2702
RT9742CGJ5-GP
1st = 074.09742.0A9F
2nd = 074.03553.007F
3rd = 074.07115.009F
4th = 074.06288.007B
PIN#4 Vin_high 1.5V
PCH_MS_EN_R
C2719
C2720
SC4D7U6D3V2MX-GP-U
0917 -SB
U2702 change to 074.51712.009F
add 2nd 074.03553.007F
add 3rd 074.09742.0A9F
by Soucer
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil
0803 -SA
1D8V_CODEC Change to 1D8V_S5 for gnd separate
by EE
U2701
ALC3314-CG-GP
1st = 071.03314.0A03
0526 -SA
Connect to APU follow ROTA1.1
by EE
0608 - SA
Delect CODEC_I2C_SCL
&CODEC_I2C_SDA
0526 -SA
Connect to APU follow ROTA1.1
by EE
0608 - SA
Remove CODEC_I2C_SCL
& CODEC_I2C_SDA
0702 - SA
add LID_CLOSE_N connect to GPIO1
by Vendor
0721 - SA
R2712 DY for Sequence
0527 -SA
Rename AMP_EAPD_N
by EE
0720 - SA
U2701.13 Change to X
0612 -SA
EC2736 DY
by EMC
1st = 068.00005.0051
2nd = 068.00006.0031
1st = 083.04024.00A1
2nd = 75.05125.070
3rd = 063.PJSD5.00A0
0624 -SA
C2707 Change to 0402 for downsize
C2708 Change to 0402 for downsize
C2703 Change to 0402 for downsize
C2736 Change to 0402 for downsize
0915 -SB
R2712 change to mount
0924 - SB
R2715 change to short pad
0720 -SA
Remove HDA_RST_N_CODEC net
201012 -SB
add Q2701 - R2718 - R2717 - R2716
20201014-SB
Add R2725
1st = 84.2N702.J31 Vgs(th) = 1~2.5V
2nd = 084.27002.0L31
3rd = 084.27002.0N31
2N7002K-2-GP-U
close to U2701.3
close to U2701.18
0624 -SA
C2735 Change to 0402 for downsize
0624 -SA
C2709 Change to 0402 for downsize
C2711 Change to 0402 for downsize
C2712 Change to 0402 for downsize
0624 -SA
C2718 Change to 0402 for downsize
0902 -SB
C2718 10uF change to 0.22uF
by Vendor
Digital GND & AUD_AGND
Tie Analog GND and Digital GND
under codec by a single point
audio ground must be connect to
digital ground with an 80 mil copper
bridge located directly under codec
to prevent ESD latch up.
PC BEEP
0619 -SA
R2710 Change to 1kR
by Vendor
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
027_Audio (Codec_ALC3314-CG)
13" CS ZURG Lucienne
-1
Wednesday, March 24, 2021
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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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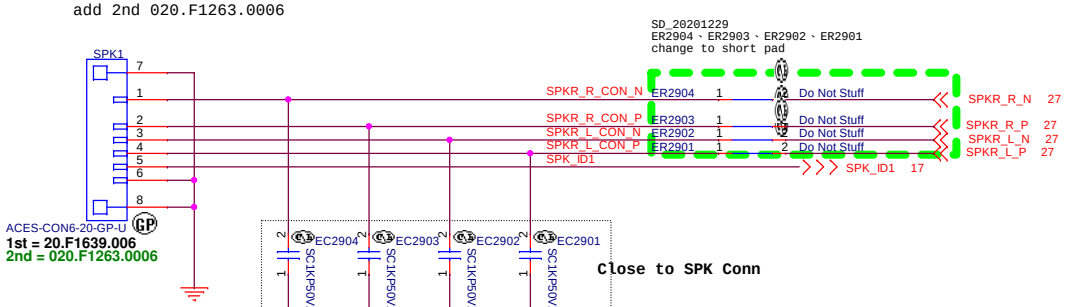
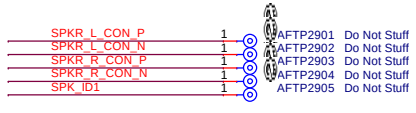
Audio_Speaker

0807 - SA
SPK1 modifiy pin define for following 14"&15"
by EE
0903 -SB
add 2nd 020.F1263.0006

Speaker vendor	VECO	Sable
SPK_ID (0 or 1)	0	1

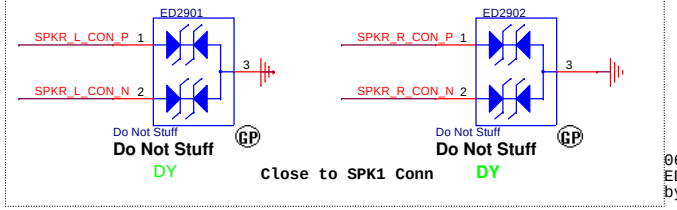


Close to SPK Conn



AFTP PLACE CLOSE TO SPK1

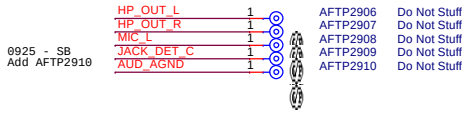
0612 - SA
EC2901~EC2904 DY
by EMC
0922 - SB
EC2901~EC2904 mount
by EMC



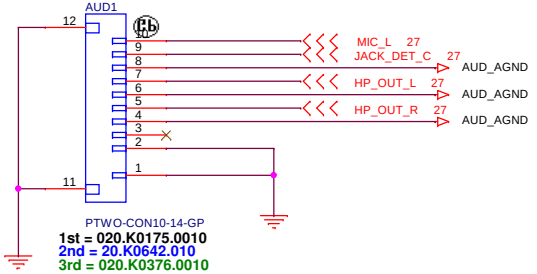
0612 - SA
ED2901~ED2902 DY
by EMC

Audio_Jack

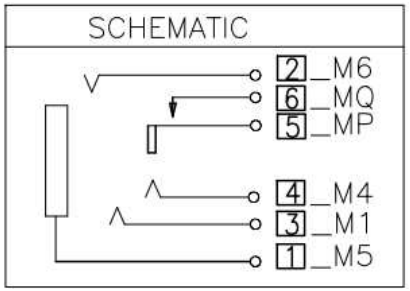
Combo-Jack (Headphone & MIC)

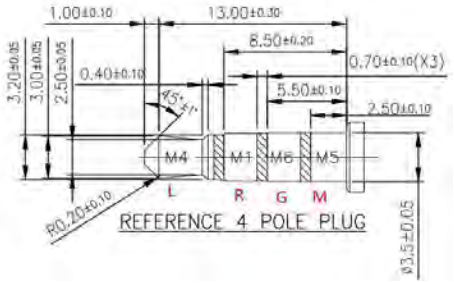


0925 - SB
Add AFTP2910



0820 - SA
AUD1 swap pin define
by ME
0903 - SB
add 2nd 20.K0642.010
add 3rd 020.K0376.0010





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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (HP/SPK/MIC Jack)
Size: A3
Document Number: 13" CS ZURG Lucienne
Rev: -1
Date: Wednesday, March 24, 2021
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https://realschematic.com

A01

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size: A2	Document Number: **13" CS ZURG Lucienne**
Rev: -1	
Date: Wednesday, March 24, 2021	Sheet 30 of 106

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https://realschematic.com

A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN (RSVD)***

Size	Document Number	Rev
A3	**13" CS ZURG Lucienne**	-1

Date: Wednesday, March 24, 2021 Sheet 31 of 106

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https://realschematic.com

A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN (RSVD)***

Size	Document Number	Rev
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Date: Wednesday, March 24, 2021 Sheet 32 of 106

SSID = Card Reader

Impedance: 50 ohm 10%

0526 -SA
Rename SD_CD_N_R

SD_20201229
ER3301
ER3302
ER3303
ER3304
ER3305
change to short pad

SD_CD_N_R — ER3301 — Do Not Stuff — SD_CD_N
SP1_R — ER3302 — Do Not Stuff — SD_D1
SP2_R — ER3303 — Do Not Stuff — SD_D0
SP4_R — ER3304 — Do Not Stuff — SD_CMD
SP5_R — ER3305 — Do Not Stuff — SD_D3
SP3_R — ER3306 — Do Not Stuff — SD_CLK
SP6_R — ER3307 — Do Not Stuff — SD_D2
SP7_R — ER3308 — Do Not Stuff

SD 0612 -SA
EC3314 DY
by ESC
DY EC3314 Do Not Stuff

SD_20201229
ER3307、ER3308
change to short pad

Modern Standby CIRCUIT

3D3V_S5 — DY_MS C3313 Do Not Stuff

0608 -SA
Change to 0R3J
R3314 Do Not Stuff
SD_20201229
R3314
change to short pad

3D3V_CR — DY_MS C3315 Do Not Stuff

CARD1_3V3: Current 800 mA

CARD1_3V3
C3311 C3312 Do Not Stuff

CARD1
SD_D0 SD_D1 SD_D2 SD_D3 SD_CD_N
VDD DAT0 DAT1 DAT2 CD/DAT3 CD CLK CMD VSS GND GND
SD_CLK SD_CMD
SKT-SDCARD-67-GP-U

SD
1st = 062.10002.0481

0817 -SA
Card1 change to 062.10002.0481
by ME

17 CARD_WAKE_N

3D3V_S5 — DY R3305 Do Not Stuff — CARD_WAKE_N

0526 -SA
Rename SD_CD_N_R
SD_CD_N_R
SP7_R
3D3V_S0_GPIO
R3301 Do Not Stuff

3D3V_S0: Current 1.2A

3D3V_S5 — C3301 C3304 Do Not Stuff

close to U301

AV12 — C3302 C3303 Do Not Stuff

Impedance: 85 ohm 10%

U3301

16	CARD_CLKREQ_CPU_N	PERST#
3	CARD_PCIE_TX_P	CLK_REQ#
3	CARD_PCIE_TX_N	HSIP
16	CARD_CLK_CPU_P	HSIN
16	CARD_CLK_CPU_N	REFCLKP
3	CARD_PCIE_RX_P	REFCLKN
3	CARD_PCIE_RX_N	HSOP
		HSON
		GND

PLT_RST_N_CR_R
CARD_PCIE_RX_P_C — C3306 Do Not Stuff
CARD_PCIE_RX_N_C — C3307 Do Not Stuff

WAKE# MS_INS# SD_CD# SP7 GPIO 3V3AUX NC#26 NC#25
NC#24 NC#23 NC#22 SP6 SP5 SP4 DV33_18 SP3
REF AV12 3V3_IN CARD_3V3 NC#13 DV12S SP1 SP2

Do Not Stuff

SP6_R SP5_R SP4_R DV33_18 SP3_R
C3305 Do Not Stuff

0601 -SA
Remove AFTP

CARD1_3V3
SD_D0 SD_D1 SD_D2 SD_D3 SD_CLK SD_CMD SD_CD_N
AFTP3301 AFTP3302 AFTP3303 AFTP3304 AFTP3305 AFTP3306 AFTP3307 AFTP3308 AFTP3309
Do Not Stuff

AFTP PLACE CLOSE TO CARD1

R3304 RREF Do Not Stuff
SP2_R SP1_R AV12
C3308 Do Not Stuff
CARD1_3V3
3D3V_S5
C3309 C3310 Do Not Stuff

0624 -SA
C3310 Change to 0402 for downsize

3D3V_CR — SD_MS RN3301 Do Not Stuff

CARD_WAKE_N
PLT_RST_N_CR_R

R3302 DY Do Not Stuff
SD_MS D3301A
1st = 83.R5003.H8H
2nd = 83.R5003.T8F
3rd = 83.R5003.I8F
Do Not Stuff
PLT_RST_N 17,39,61,63,68,89,91

D3302A Do Not Stuff
SD_MS
1st = 83.R5003.H8H
2nd = 83.R5003.T8F
3rd = 83.R5003.I8F
PLT_RST_N_CR 24

R3303 DY Do Not Stuff

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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CardReader (IC+Reader Conn)**
Size: A3
Document Number: **13" CS ZURG Lucienne**
Rev: -1
Date: Wednesday, March 24, 2021
Sheet 33 of 106

TBD

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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size: A3 | Document Number: **13" CS ZURG Lucienne** | Rev: **-1**

Date: Wednesday, March 24, 2021 | Sheet 34 of 106

USB Type A Connector

0612 -SA
Change to 4pin CMC
By RF

FR3501 Do Not Stuff
FR3502 Do Not Stuff

18 USB1_USB30_RX_N
18 USB1_USB30_RX_P
USB1_USB30_RX_CMC_N
USB1_USB30_RX_CMC_P
C3507 SCD33U6D3V2KX-1-GP
C3508 SCD33U6D3V2KX-1-GP

ED3502
USB1_USB30_RX_CON_N1
USB1_USB30_RX_CON_P1
USB1_USB30_TX_CON_N1
USB1_USB30_TX_CON_P1
AZ1043-04F-R7G-GP
1st = 075.01043.0073
2nd = 075.08809.0073

0612 -SA
Change to 4pin CMC
By RF

FR3503 Do Not Stuff
FR3504 Do Not Stuff

18 USB1_USB30_TX_N
18 USB1_USB30_TX_P
USB1_USB30_TX_CMC_N
USB1_USB30_TX_CMC_P
C3501 SCD22U10V2KX-L1-GP
C3506 SCD22U10V2KX-L1-GP

5V_USB30_1
AFTP3501 Do Not Stuff
AFTP3502 Do Not Stuff
AFTP3507 Do Not Stuff
AFTP3508 Do Not Stuff
USB1_USB20_CON_PN1
USB1_USB20_CON_PP1

AFTP PLACE CLOSE TO USB1

0527 -SA
Rename USB1_USB20_N

18 USB1_USB20_N
18 USB1_USB20_P
EL3501
FILTER-4P-132-GP
USB1_USB20_CON_PN1
USB1_USB20_CON_PP1
1st = 68.02002.061
2nd = 068.09002.2001

0527 -SA
Rename USB1_USB20_P

0612 -SA
ER3503/ER3504 DY
By EMC
0922 - SB
Remove ER3503/ER3504
By EE

ED3501
I/O1 I/O4
GND VDD
I/O2 I/O3
AZC099-04S-2-GP
1st = 075.09904.0A7C
2nd = 75.00199.07C

5V_USB30_1
R3520
0R2J-2-GP
ED3501_VCC
0710 -SA
R3520 change to SMD type

0624 -SA
C3514 Change to 0402 for downsize
C3527 Change to 0402 for downsize

Gen1
USB3.2 Standard
(Left side)

5V_USB30_1
C3502 SCD22U6D3V3MX-L1-GP
C3503 SCD22U6D3V3MX-L1-GP
C3504 Do Not Stuff
C3505 Do Not Stuff
DY DY

USB1
VBUS
D+
D-
STDA_SSRX+
STDA_SSRX-
STDA_SSTX+
STDA_SSTX-
GND
USB1_USB20_CON_PP1
USB1_USB20_CON_PN1
SKT-USB13-565-GP-U
1st = 022.10005.0NM1

0603 -SA
USB1 change for emn
0817-SA
USB1 change to 022.10005.M081
by ME
0819-SA
USB1 change to 022.10005.0NM1
by ME

2A
Active high

5V_S5
5V_USB30_1
U3501
VIN
VOUT
GND
EN/EN#
FLG#
24 USB_PWR_EN
PIN#4 Vin_high 1.5V
RT9742CGJ5-GP
C3514 C3527
SCD10U6D3V2MX-GP-U
R3521
100KR2J-4-GP
1st = 074.09742.0A9F
2nd = 074.03553.007F
3rd = 074.07115.009F
4th = 074.06288.007B

0917 -SB
U3501 change to 074.51712.009F
add 2nd 074.03553.007F
add 3rd 074.09742.0A9F
by Soucer

USB Type A Connector

0612 -SA
Change to 4pin CMC
By RF

FR3505 Do Not Stuff
FR3506 Do Not Stuff
SD_20201230
FR3505、FR3506
change to short pad

18 USB3_USB30_RX_N
18 USB3_USB30_RX_P
USB3_USB30_RX_CMC_N
USB3_USB30_RX_CMC_P
C3528 SCD33U6D3V2KX-1-GP
C3529 SCD33U6D3V2KX-1-GP

ED3503
USB3_USB30_RX_CON_N1
USB3_USB30_RX_CON_P1
USB3_USB30_TX_CON_N1
USB3_USB30_TX_CON_P1
AZ1043-04F-R7G-GP
1st = 075.01043.0073
2nd = 075.08809.0073

0612 -SA
Change to 4pin CMC
By RF

FR3507 Do Not Stuff
FR3508 Do Not Stuff
SD_20201230
FR3507、FR3508
change to short pad

18 USB3_USB30_TX_N
18 USB3_USB30_TX_P
USB3_USB30_TX_CMC_N
USB3_USB30_TX_CMC_P
C3540 SCD22U10V2KX-L1-GP
C3541 SCD22U10V2KX-L1-GP

5V_USB30_3
AFTP3503 Do Not Stuff
AFTP3504 Do Not Stuff
AFTP3509 Do Not Stuff
AFTP3510 Do Not Stuff
USB3_USB20_CON_PN1
USB3_USB20_CON_PP1

AFTP PLACE CLOSE TO USB3

0527 -SA
Rename USB3_USB20_N

18 USB3_USB20_N
18 USB3_USB20_P
EL3502
FILTER-4P-132-GP
USB3_USB20_CON_PN1
USB3_USB20_CON_PP1
1st = 68.02002.061
2nd = 068.09002.2001

0527 -SA
Rename USB3_USB20_P

0612 -SA
ER3501/ER3502 DY
By EMC
0922 - SB
Remove ER3501/ER3502
By EE

ED3504
I/O1 I/O4
GND VDD
I/O2 I/O3
AZC099-04S-2-GP
1st = 075.09904.0A7C
2nd = 75.00199.07C

5V_USB30_3
R3523
0R2J-2-GP
ED3504_VCC
0710 -SA
R3523 change to SMD type

0624 -SA
C3530 Change to 0402 for downsize
C3531 Change to 0402 for downsize

Gen1
USB3.2 Standard
(Right side)

5V_USB30_3
C3535 Do Not Stuff
C3534 SCD22U6D3V3MX-L1-GP
C3533 Do Not Stuff
C3532 SCD22U6D3V3MX-L1-GP
DY DY

USB3
VBUS
D+
D-
STDA_SSRX+
STDA_SSRX-
STDA_SSTX+
STDA_SSTX-
GND
USB3_USB20_CON_PP1
USB3_USB20_CON_PN1
SKT-USB13-565-GP-U
1st = 022.10005.0NM1

0603 -SA
USB3 change for emn
0817-SA
USB3 change to 022.10005.M081
by ME
0819-SA
USB1 change to 022.10005.0NM1
by ME

2A
Active high

5V_S5
5V_USB30_3
U3502
VIN
VOUT
GND
EN/EN#
FLG#
USB_PWR_EN
PIN#4 Vin_high 1.5V
RT9742CGJ5-GP
C3531 C3530
SCD10U6D3V2MX-GP-U
R3522
100KR2J-4-GP
1st = 074.09742.0A9F
2nd = 074.03553.007F
3rd = 074.07115.009F
4th = 074.06288.007B

0917 -SB
U3502 change to 074.51712.009F
add 2nd 074.03553.007F
add 3rd 074.09742.0A9F
by Soucer

A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB3.0 Conn)

Size	Document Number	Rev
A3	13" CS ZURG Lucienne	-1

Date: Wednesday, March 24, 2021 Sheet 35 of 106

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USB Charger IC

0527 -SA
Remove USB Charger

TBD

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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB Charger)

Size: A3 | Document Number: 13" CS ZURG Lucienne | Rev: -1

Date: Wednesday, March 24, 2021 | Sheet 36 of 106

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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB (RSVD)**

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USB 3.0 Redriver_MB

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB (USB3.0 Redriver/USB2.0 Hub)

Size	Document Number	Rev
A3	13" CS ZURG Lucienne	-1

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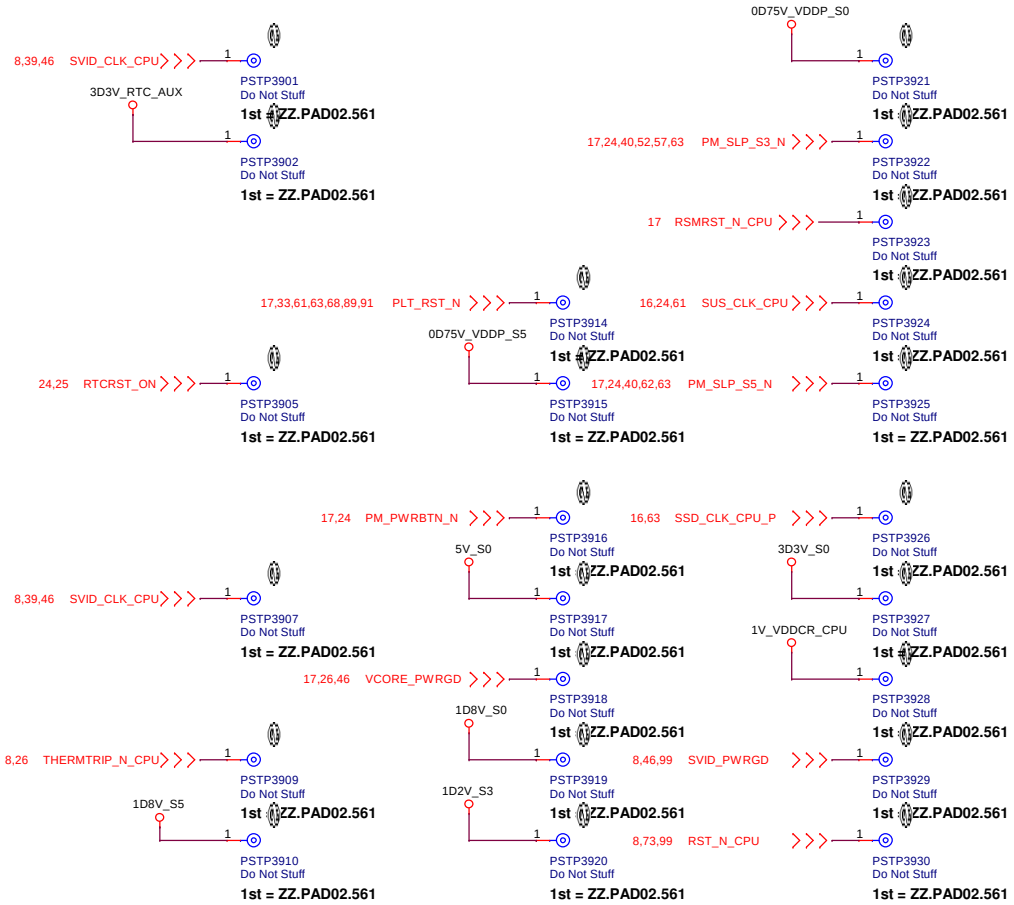

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A01

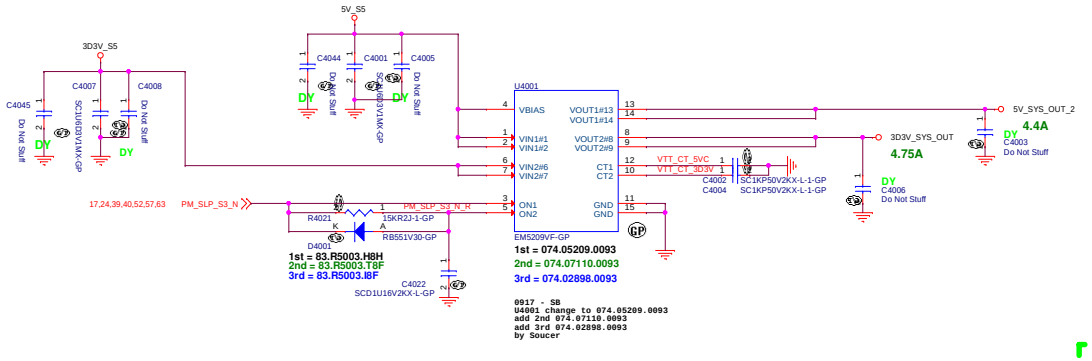
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

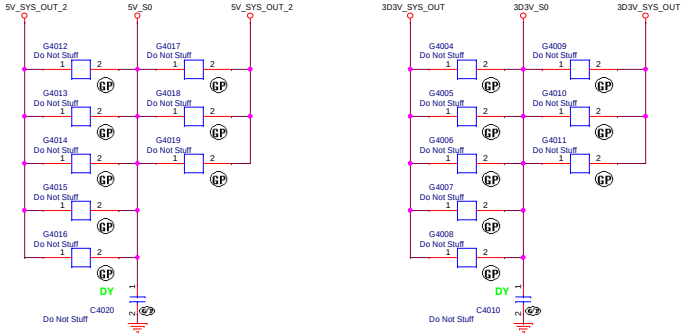
Title: ***R360 Test Point***

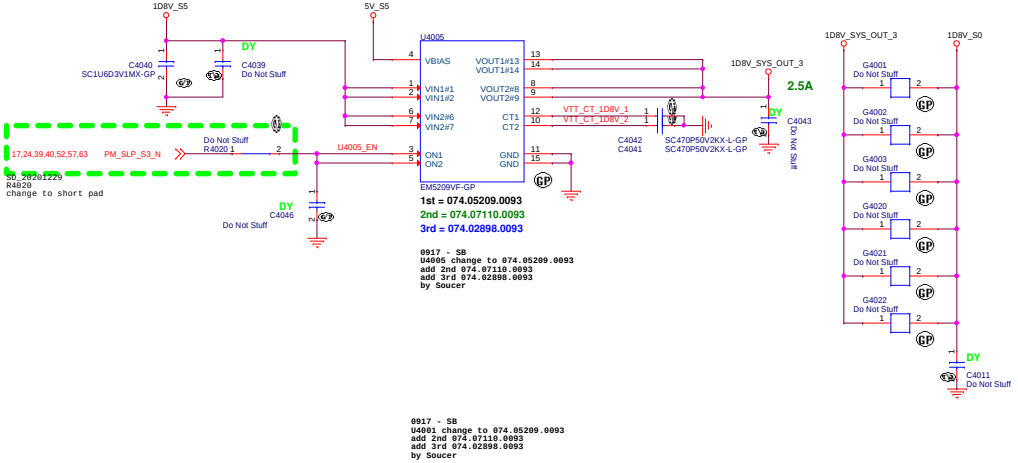
Size: A3 | Document Number: **13" CS ZURG Lucienne** | Rev: -1

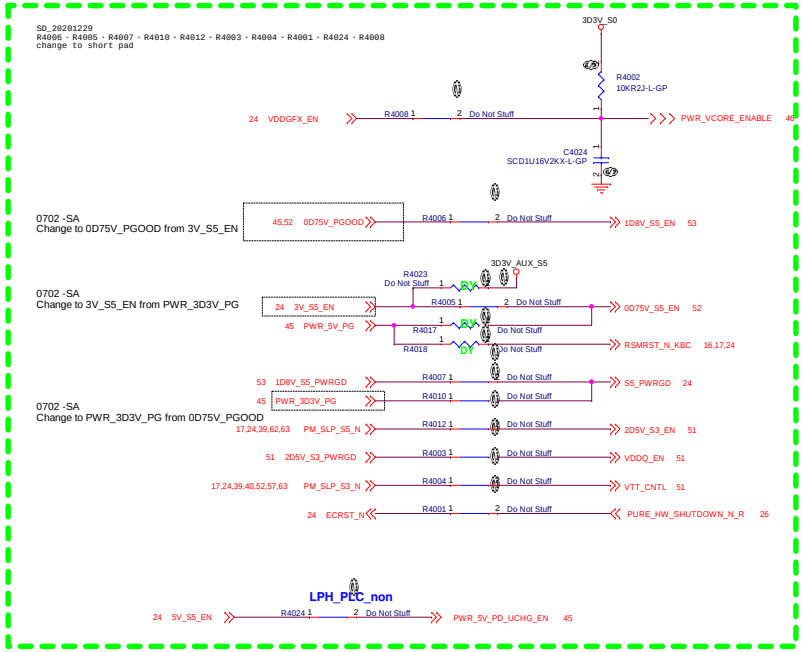
Date: Wednesday, March 24, 2021 | Sheet 39 of 106

Run Power Sequence









Discharge Circuit

0608 - SA
Remove Discharge
by EE

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A01

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Sequence (Power Plane Enable)*		
Size: A2	Document Number: 13" CS ZURG Lucienne	Rev: -1
Date: Wednesday, March 24, 2021	Sheet 40 of 106	

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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Sequence (RSVD)

Size	Document Number	Rev
A4	**13" CS ZURG Lucienne**	-1
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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***INT IO (RSVD)***

Size	Document Number	Rev
A4	**13" CS ZURG Lucienne**	-1

Date: Wednesday, March 24, 2021 Sheet 42 of 106

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Battery Connector

Check Battery Pin Spec

0707 - SA
R4301 changes to SMD type
0924 - SB
R4301 changes to short pad

Main Battery

KBC Power

1st = 83.R5003.HBH
2nd = 83.R5003.T8F
3rd = 83.R5003.8F

1st = 83.R5003.HBH
2nd = 83.R5003.T8F
3rd = 83.R5003.8F

0903 - SB
BATT1 add 2nd 020.F1198.0010

1st = 020.F1196.0010
2nd = 020.F1198.0010

1st = 83.05725.0A0

Pin No.	Symbol	Comments
1,2	GND	Batt-, Battery Negative Terminal
3	B/I	Connected to GND.
4,5,6	BATT+	Batt+, Battery Positive Terminal.
7	RTC	LDO – 3.3V (see Note 7)
8	SMD	SMBus data interface I/O pin.
9	SMC	SMBus clock interface I/O pin
10	GND	Batt-, Battery Negative Terminal

Table 4. Function table for asynchronous operation[5]

Input				Output	
SD	RD	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 5. Function table for synchronous operation[1]

Input				Output	
SD	RD	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

RFQ_190904
add common part(2nd/3rd)

1st = 84.05212.B1Y
2nd = 84.00126.H1K
3rd = 084.00024.0B1K

1st = 73.01G74.0HB
2nd = 73.01G74.007

1st = 075.09904.0A7C
2nd = 75.00199.07C

1st = 84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.27002.0N31

Vgs(th) = 1~2.5V

1st = 75.00054.T7D
2nd = 75.00054.A7D
3rd = 075.00054.0B7D

8623 -SA
New Storage mode circuit

SC-20201124
Q4305 Change Commom (Same as Mel)

1st = 84.00084.E31
2nd = 84.00084.P31
3rd = 084.00841.0031

O_STM -> original storage mode
N_STM -> new storage mode

8915 - SB
RN4301 change to 2k2 from 100k

20201014-SB
1.RN4301 change to 100k from 2K2
_SIV 量測波型太醜更換阻值
2.ADD C4304

1st = 75.27002.F7C
2nd = 075.27002.0E7C

Vgs(th) = 1.0~2.5V

RFQ_190610
move to P.44

DCIN Connector

0807 - SA
DCIN1.7 & DCIN1.8 change to NC
0903 - SB
add 2nd 020.F008L.0008
add 3rd 020.F1297.0008
SC-20201111
Remove 020.F0323.0008
Remove 020.F1297.0008
add 1st 020.F08C.0008
add 2nd 020.F006L.0008

EMI ?PWR?

1st = 083.04024.00A1
2nd = 70.05125.071
3rd = 083.PJ5D5.00A0

EMI ?PWR?

1st = 83.P6SM8.AAG
2nd = 083.00020.00AG

8716 - SA
C4301 Change 0603 for common part

1st = 020.F000C.0008
2nd = 020.F000L.0008

AFTP test point

AC Present = White
Standby = White pulsing
Charging = Amber
*LED's are off if no AC jack pluged in

8723 - SA
PR4311 & PR4312 Change to DY
0908 - SB
Net DC_BATFULL & CHARGE_LEC Swap

-1_20200831"
add R4338 ~ R4339 於 CHARGE_LED 一結端同時一下

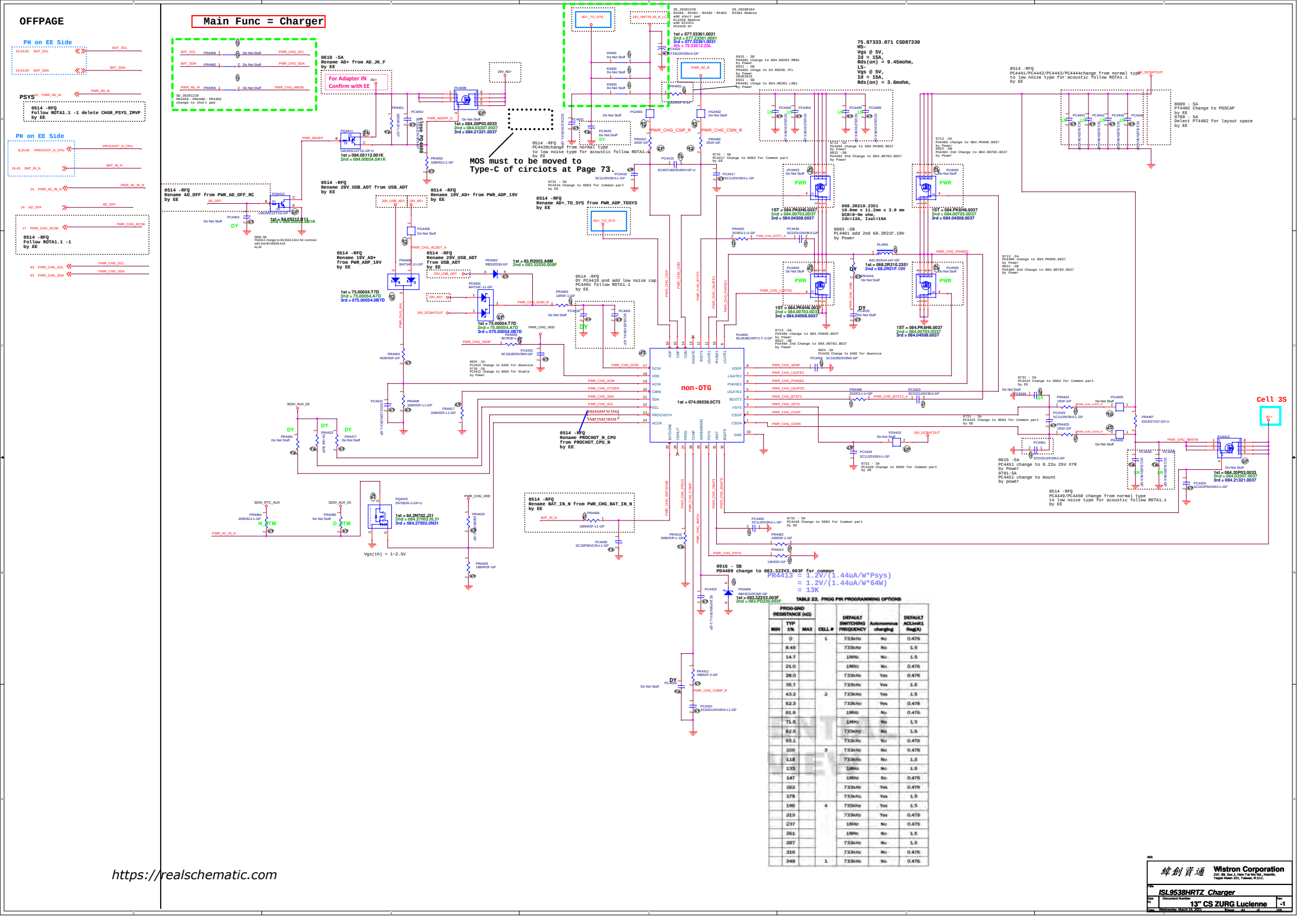
Main Func = ADT Input

0603 - SA
Add Charge LED circuit
0611 - SA
LED2 Change to 83.00326.A70
By ME
0813 - SA
LED2 change to 83.00326.G70
by ME

1st = 83.00326.G70

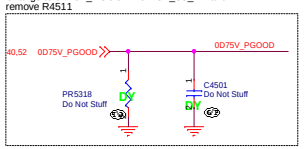
https://realschematic.com

Wistron Corporation	22F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: INT IO (ATX/ DC/ BATT Conn)			
Size: A1	Document Number: 13" CS ZURG Lucienne		Rev: -1
Date: Wednesday, March 24, 2021	Sheet: 43 of 106		

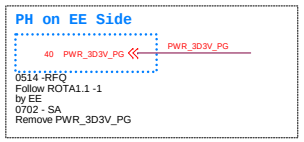

OFFPAGE
Main Func = Charger
PH on EE Side
PSYS
PH on EE Side
0514 -RFQ Follow ROTA1.1 -1 delete CHGR_PSYS_INVP by EE
0610 -SA Rename AD+ from AD_JK_F by EE
For Adapter IN Confirm with EE
MOS must to be moved to Type-C of circiots at Page 73.
non-OTG
Cell 3S
0916 - SB PD4409 change to 083.32V3.003F for common
PR4413 = 1.2V/(1.44uA/W*Psys)
= 1.2V/(1.44uA/W*64W)
= 13K
TABLE 22. PROG PIN PROGRAMMING OPTIONS
https://realschematic.com
Wistron Corporation
ISL9538HRTZ Charger
13" CS ZURG Luclenne

OFFPAGE-Signal

0514 -RFQ
Follow ROTA1.1 -1
by EE
0702 -SA
Change to 0D75V_PGOOD from 3V_S5_EN and remove R4511



PH on EE Side

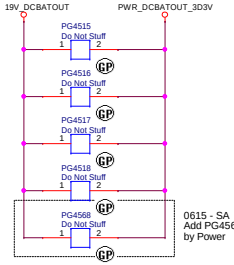


0514 -RFQ
Follow ROTA1.1 -1
by EE
0702 - SA
Remove PWR_3D3V_PG

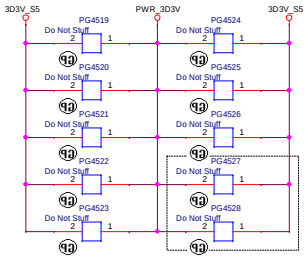
0514 -RFQ
Rename PWR_5V_PD_UCHG_EN from PWR_5V_EN
by EE

0514 -RFQ
Follow ROTA1.1
by EE

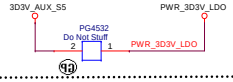
OFFPAGE-GAP

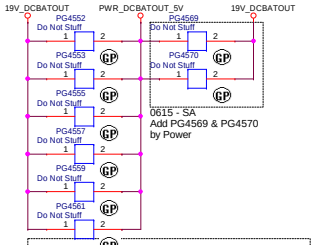


0615 - SA
Add PG4568
by Power

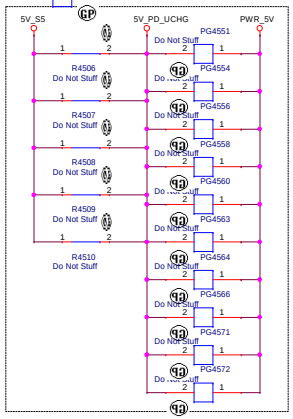


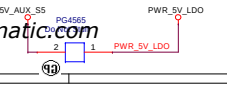
0514 -RFQ
Add PG4527 & PG4528
by EE



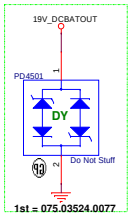


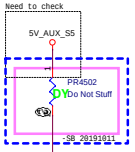
0615 - SA
Add PG4569 & PG4570
by Power



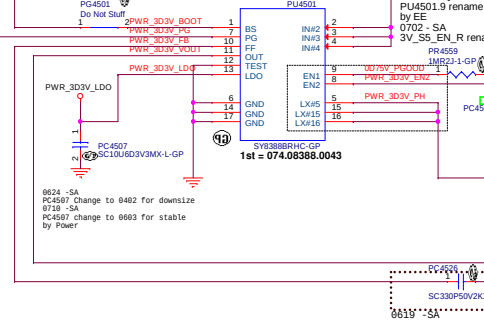


SY8388BR 3D3V

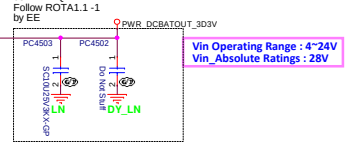




Place another side , make GND plan bigger

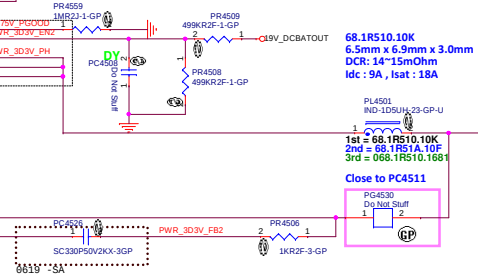


0514 -RFQ
PU4501.9 rename 3V_S5_EN_R
by EE
0702 - SA
3V_S5_EN_R rename 0D75V_PGOOD



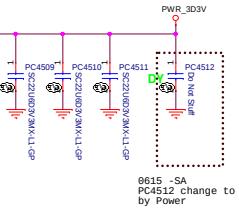
Vin Operating Range : 4~24V
Vin_Absolute Ratings : 28V

EN1 & EN2 Rating : IN +0.3V
EN2/EN1 Rising Threshold : 1.0V
EN2/EN1 Falling Threshold : 0.4V



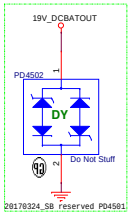
68.1R510.10K
6.5mm x 6.9mm x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

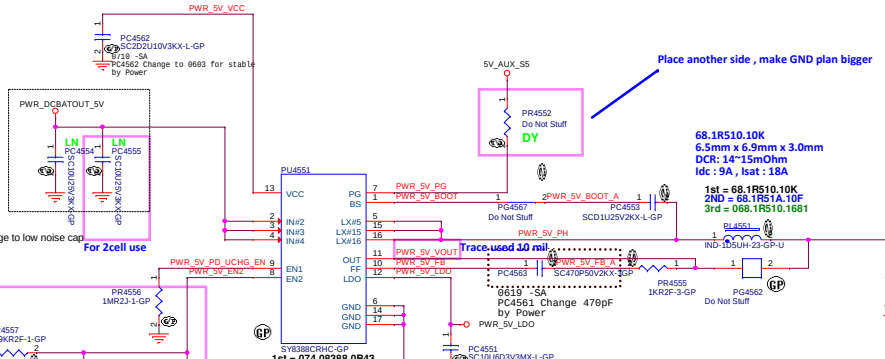
IDC : 8A
OCP : 10A



0615 -SA
PC4512 change to DY
by Power

SY8388C 5D0V





0514 -RFQ
PC4554 & PC4555 change to low noise cap
follow ROTA1.1 -1
by EE

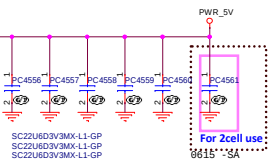
Trace used 10 mil

0619 -SA
PC4561 Change 470pF
by Power

Place another side , make GND plan bigger

68.1R510.10K
6.5mm x 6.9mm x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A
1st = 68.1R510.10K
2ND = 68.1R51A.10F
3rd = 068.1R510.1681

IDC:8A



0615 -SA
PC4561 Chage to mount
by Power

0514 -RFQ
Add R4506~4508
Add Power net 5V_PD_UCHG
by EE
0615 - SA
Add PG4571 & PG4572

EN rating 25V
EN Rising Threshold : 0.8V

Ilimt : 8A

Place another side , make GND plan bigger

A01

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8386B&SY8388C_5V/3D3V

Size: A2 | Document Number: 13" CS ZURG Lucienne | Rev: -1

Date: Wednesday, March 24, 2021 | Sheet 45 of 106

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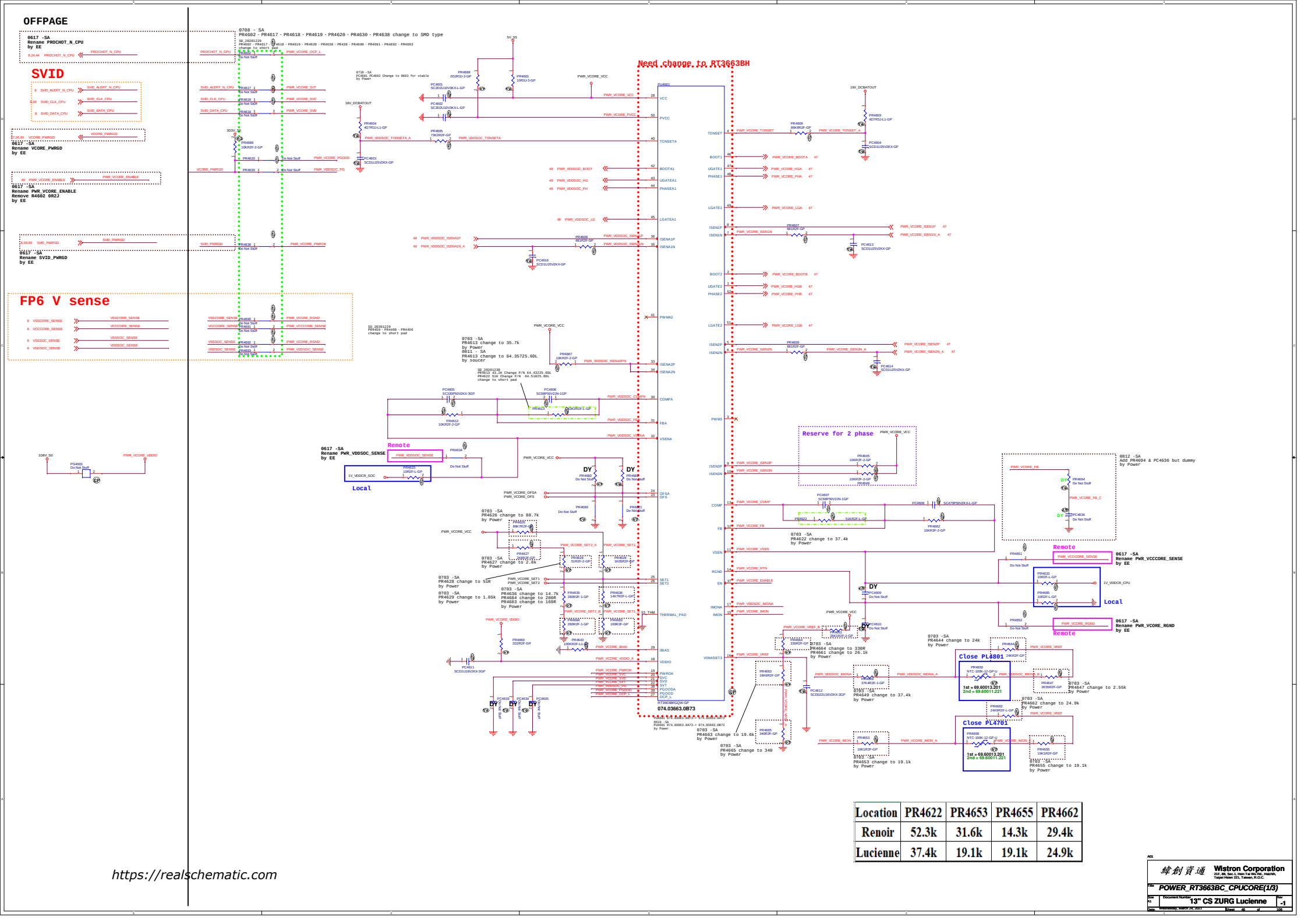

Location	PR4622	PR4653	PR4655	PR4662
Renoir	52.3k	31.6k	14.3k	29.4k
Lucienne	37.4k	19.1k	19.1k	24.9k

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: POWER_RT3663BC_CPUCORE(1/3)
Size: A1
Document Number: 13" CS ZURG Lucienne
Rev: -1
Date: Wednesday, March 24, 2021
Sheet: 46 of 106

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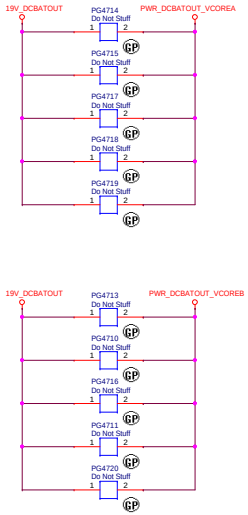
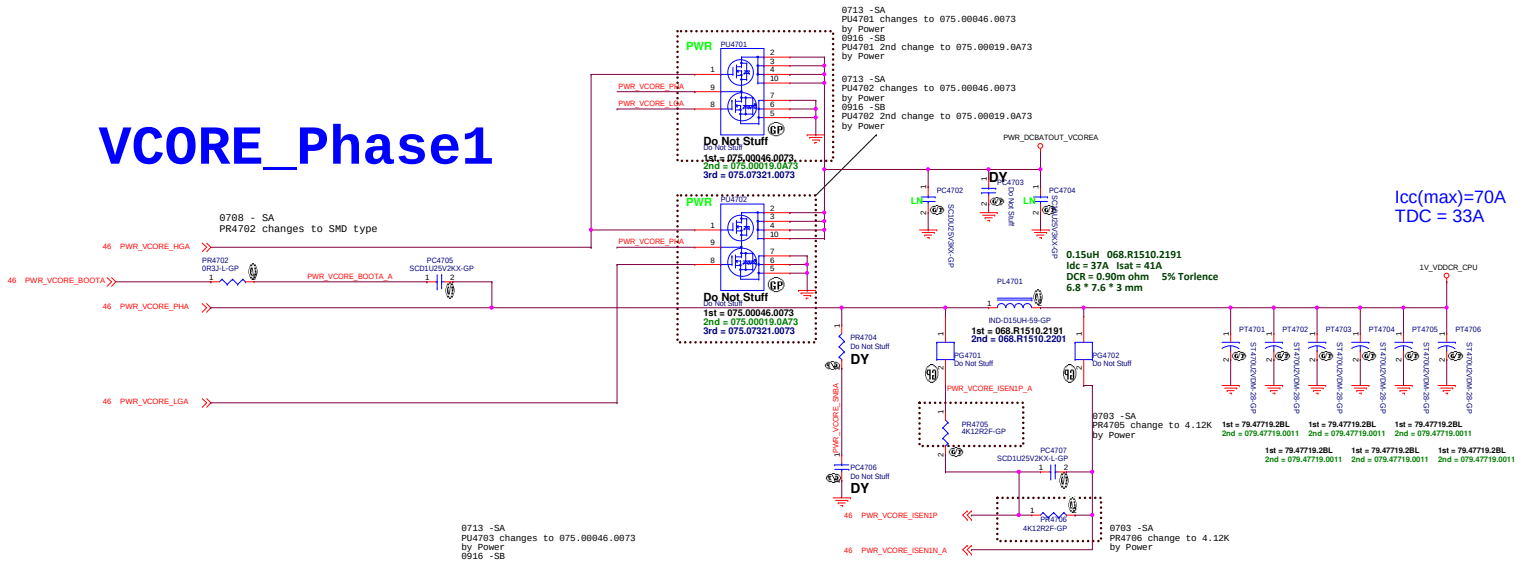
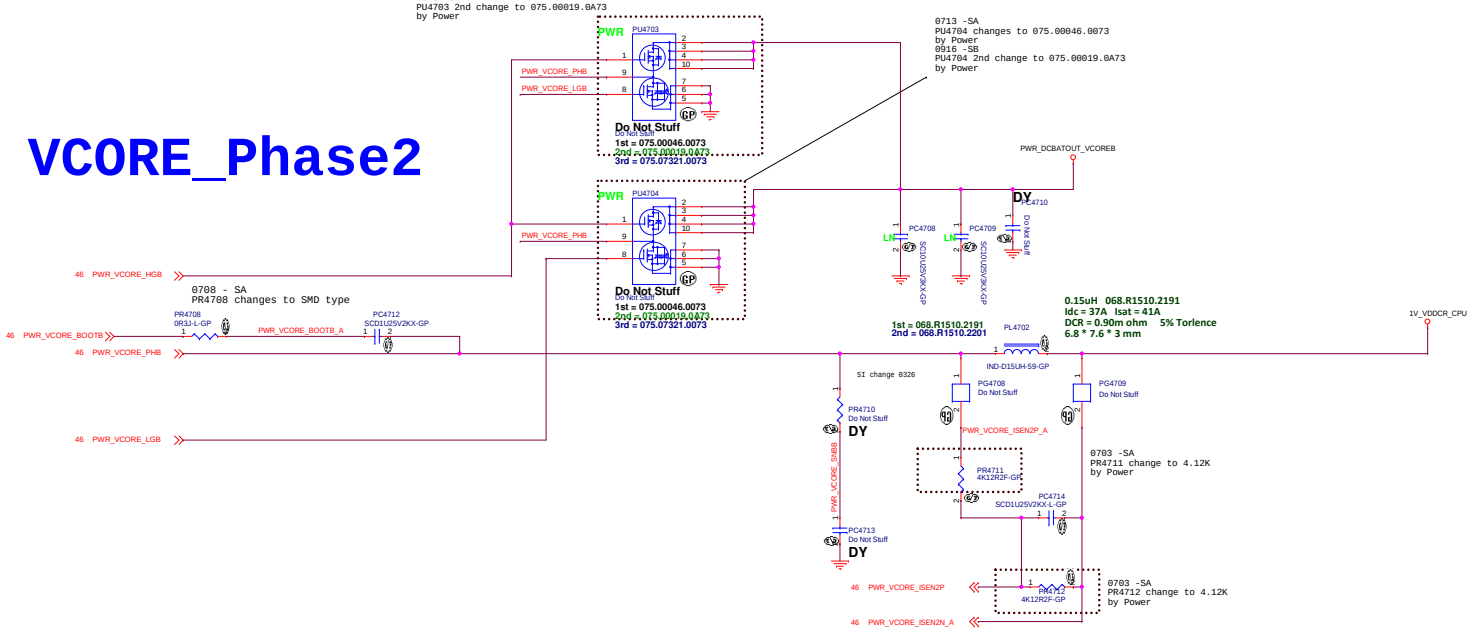


VCORE_Phase1



VCORE_Phase2



A01

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER_RT3663BC_CPUCORE(2/3)

Size: Custom | Document Number: 13" CS ZURG Lucienne | Rev: -1

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VDDSOC_Phase1

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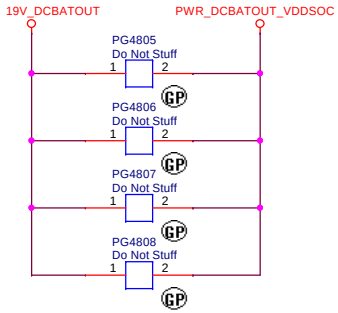
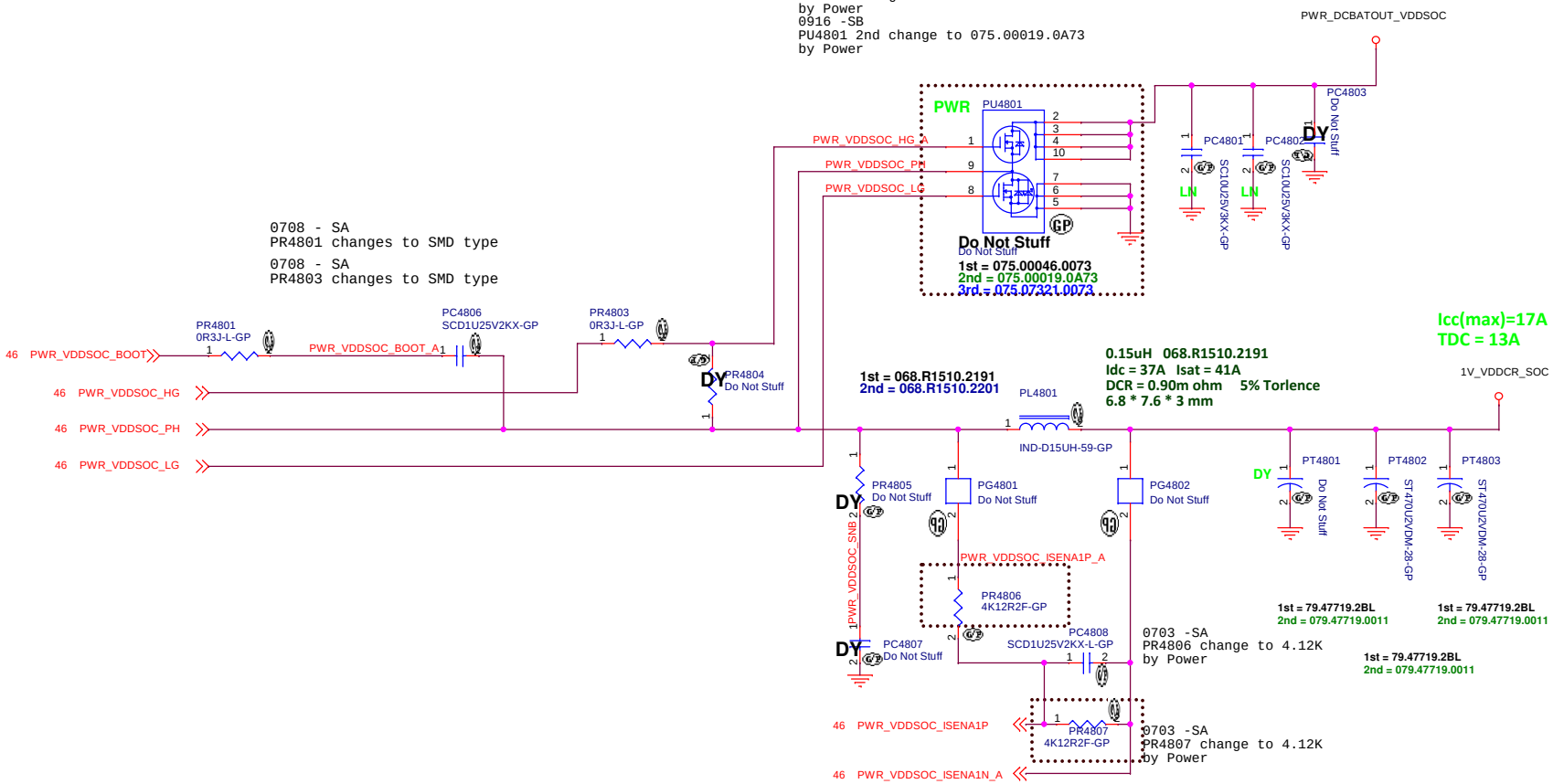


0713 -SA
PU4801 changes to 075.00046.0073
by Power
0916 -SB
PU4801 2nd change to 075.00019.0A73
by Power

0708 - SA
PR4801 changes to SMD type

0708 - SA
PR4803 changes to SMD type



A01

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Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER_RT3663BC_CPUCORE(3/3)	
Size A3	Document Number 13" CS ZURG Lucienne	Rev -1
Date: Wednesday, March 24, 2021	Sheet 48 of 106	

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A01

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Power (RSVD)***
Size: A3	Document Number: **13" CS ZURG Lucienne**
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Date: Wednesday, March 24, 2021	Sheet 49 of 106

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A01

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	***Power (RSVD)***	
Size A3	Document Number **13" CS ZURG Lucienne**	Rev **-1**
Date: Wednesday, March 24, 2021	Sheet 50 of 106	

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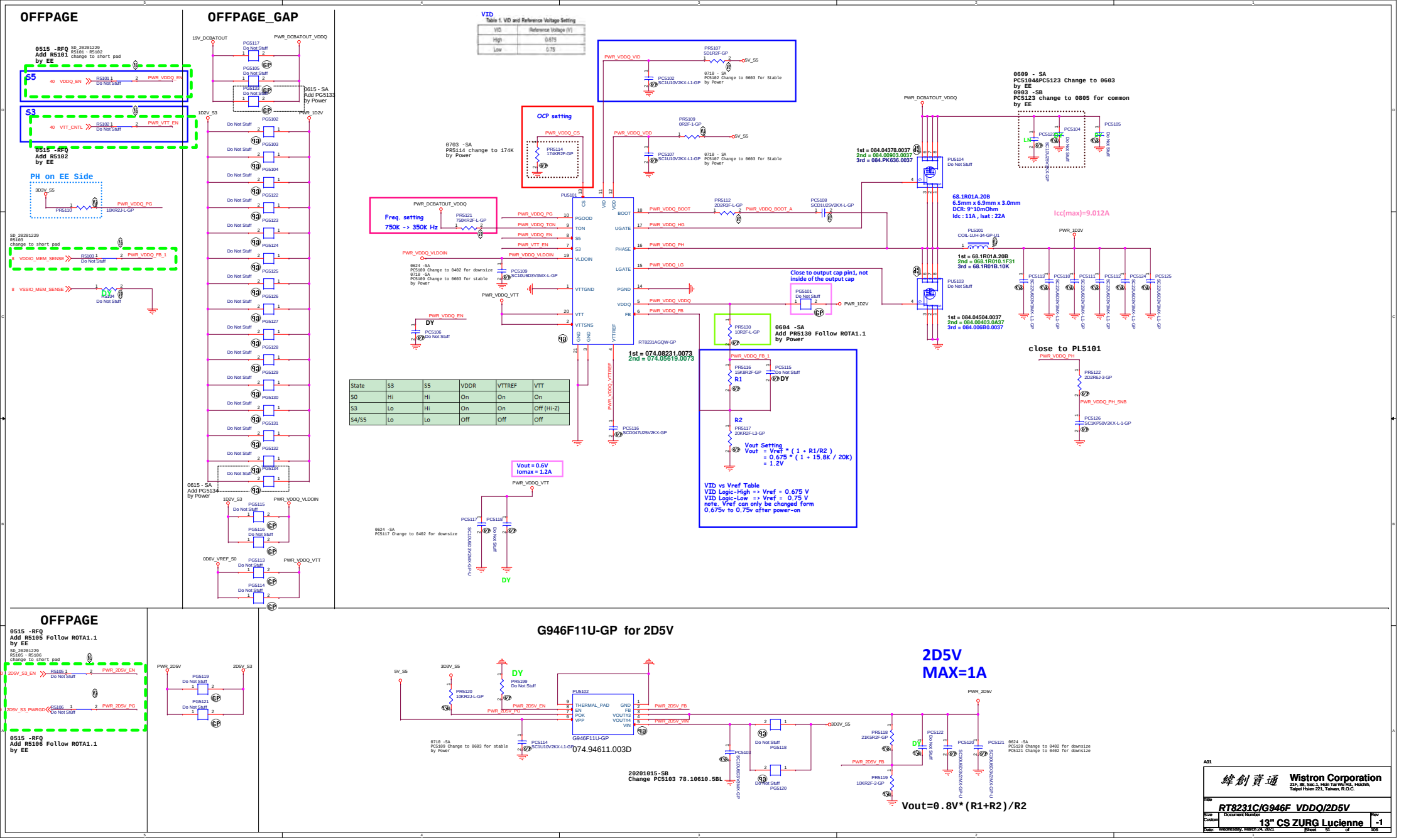

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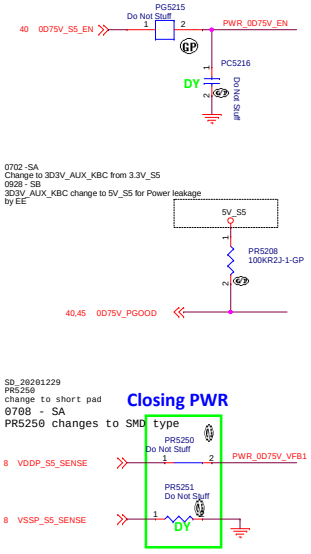

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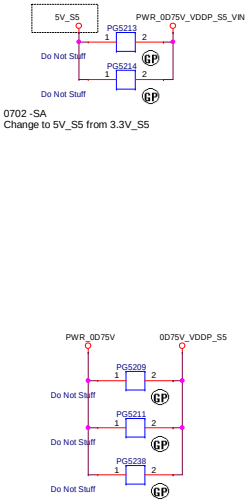
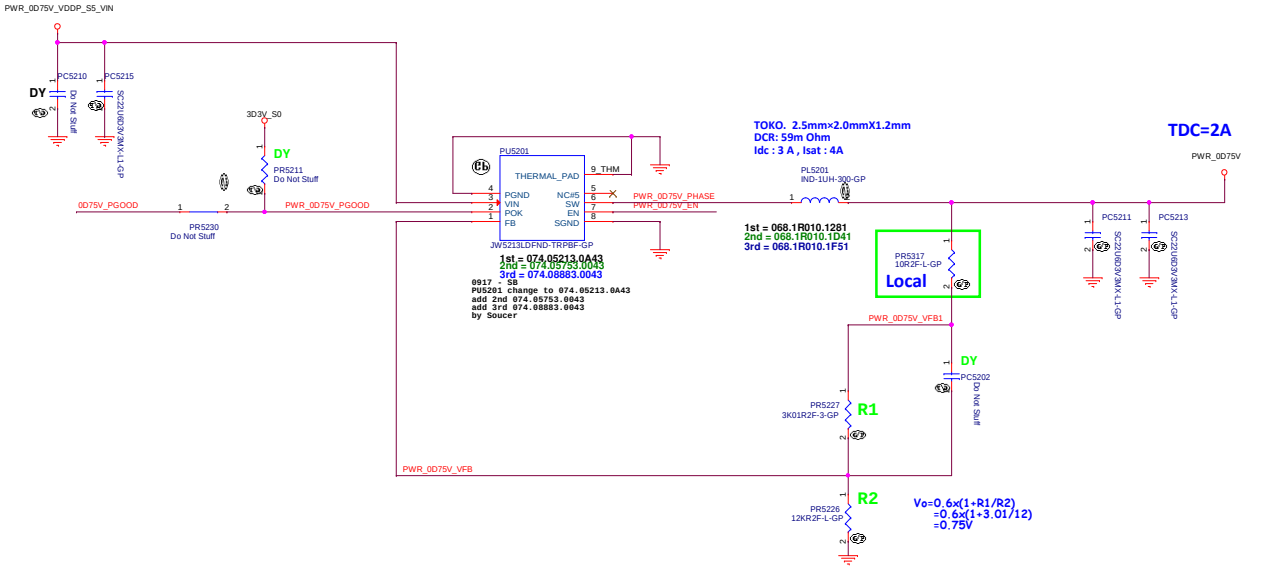


G2822D for 0D75V_S5



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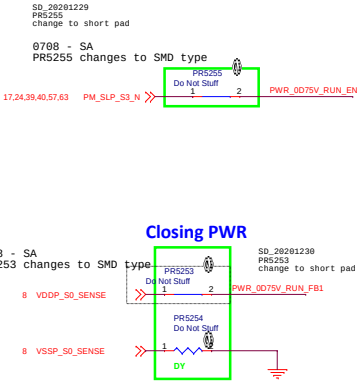

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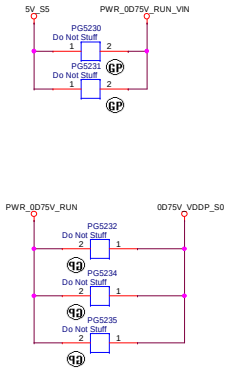
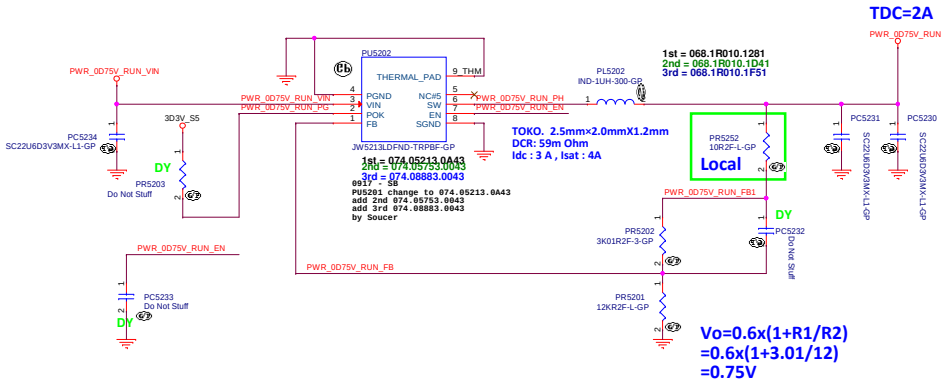


G2822D for 0D75V



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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (AOZ2262_VDDP_0D75V)

Size	Document Number	Rev
A2	13" CS ZURG Lucienne	-1

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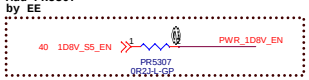
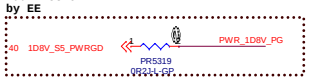
0518 -RFQ
Add PR5307
by EE



0518 -RFQ
Add PR5319
by EE



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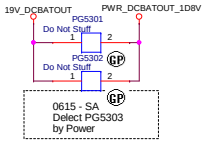
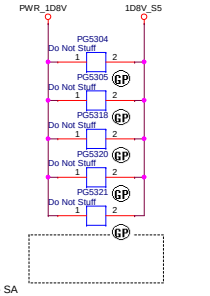
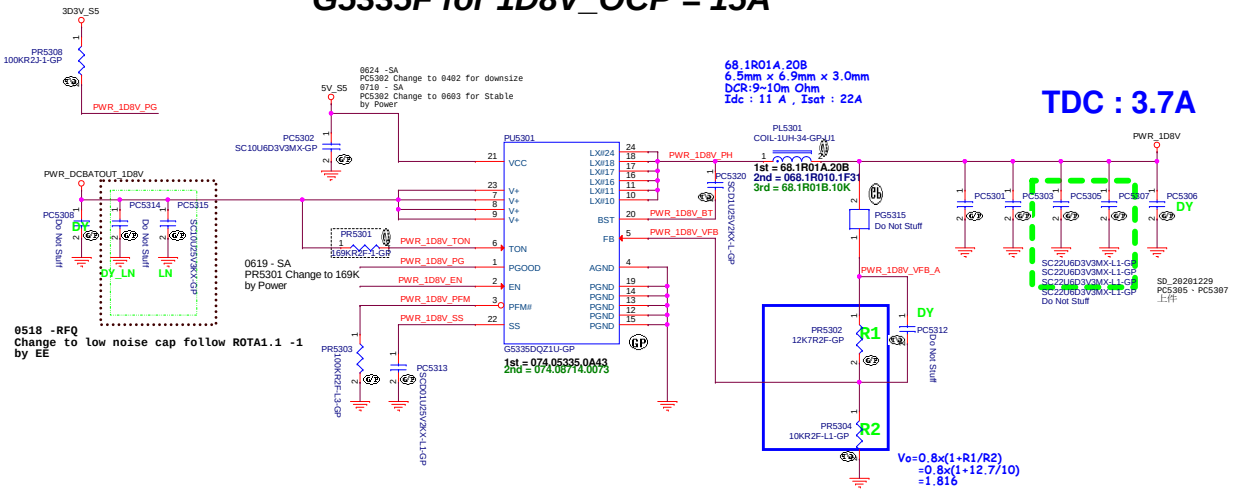




0615 - SA
Delect PG5322、PG5323、PG5316、PG5317、PG5319
by Power

SSID = PWR.Plane.Regulator_1p0v

G5335F for 1D8V_OCP = 15A



TDC : 3.7A

A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G5335F_1D8V	
Size: Custom	Document Number: 13" CS ZURG Lucienne	Rev: -1
Date: Wednesday, March 24, 2021	Sheet 53 of 106	

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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power (RSVD)

Size	Document Number	Rev
Custom	13" CS ZURG Lucienne	-1

Date: Wednesday, March 24, 2021 Sheet 54 of 106

AFTP PLACE CLOSE TO LCD1

0602 -SA
Delect CPU_I2C_SCL_SENSOR&
CPU_I2C_SDA_SENSOR

0602 -SA
Delect
3D3V_SENSORHUB_S5、5V_Touch、
I2C_SDA_TOUCH、I2C_SCL_TOUCH、
TOUCH_Report_SW_N、TOUCH_RST_N
TOUCH_5V_EN

eDP+WOV

0903 - SB
LCD1 add 2nd 20.K0809.034
add 3rd 020.K0160.0034

LCD1

LCD1.17
Pin17 GND for MIC detect (2MIC)
Pin17 NC for non-MIC (4MIC)

1st = 20.K0678.034
2nd = 20.K0809.034
3rd = 020.K0160.0034

0703 - SA
Rename DMIC2_I2C_SDA from DMIC_I2C_SDA

SD_20201230
R5541、R5531
change to short pad

R5531 closes to LCD1

SC-20201113
ADD R5540、R5541 MIC 改走1.8V 路徑
Remove R5532

C5533、C5534、F5503 closes to LCD1

1.1A
F5503
POLYSW-1D1A6V-9-GP-U
0.1A
DY_MS
C5533
1st = 69.48001.081
2nd = 69.50011.081
1.8V

0706 - SA
Add WoV power circuit

SC-20201113
Remove R5521
Add C5535、C5536、FF04

C5535、C5536、F5504 closes to CAM1

1.1A
F5504
POLYSW-1D1A6V-9-GP-U
0.5A
DY_MS
C5535
1st = 69.48001.081
2nd = 69.50011.081
1.8V

C5522、C5524、F5502 closes to CAM1

1.1A
F5502
POLYSW-1D1A6V-9-GP-U
0.5A
DY_MS
C5522
1st = 69.48001.081
2nd = 69.50011.081
3.3V

CCD

CAM1
PTWO-CON10-14-GP
1st = 020.K0175.0010
2nd = 20.K0642.010
3rd = 020.K0376.0010

SD_20201230
R5539
change to short pad

SD_20201230
R5530
change to short pad

to CPU
R5530 closes to CAM1

0603 -SA CAM1 change for emn
0618 -SA CAM1 follow Pin Define table
0903 - SB
CAM1 add 2nd 20.K0642.010
add 3rd 020.K0376.0010

SC-20201111
ADD R5538、R5539 MIC 改走1.8V 路徑

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LED BACKLIGHT CONVERTER POWER

24V/1.1A
F5501
POLYSW-1D1A24V-GP-U
1st = 69.50007.A31
2nd = 69.50007.G71

0602 -SA
Delect D5502

ED5503 closes to LCD1

ED5503
0710 - SA
add R5533
0813 - SA
R5533 Change to DY for Wlan detect
1st = 075.09904.0A7C
2nd = 75.00199.07C

ED5502 closes to CAM1

ED5502
0612 -SA
ED5502 DY
by EMC
0813 -SA
R5537 Change to DY for Wlan detect
0710 - SA
add R5537
1st = 075.09904.0A7C
2nd = 75.00199.07C

0608 -SA
Add CMC CHOKE for RF
0611 -SA
Change CMC for common part
0612 -SA
EL5501 DY
by EMC

SD_20201230
ER5509 ~ ER5510
change to short pad

0602 -SA
Change to CCD_USB20_SW_P & CCD_USB20_SW_N
from CCD_USB20_P & CCD_USB20_N

-1_20200319
Remove EL5501

1st = 75.05125.07D
2nd = 075.52215.007D
3rd = 075.05011.007D

0716 -SA
Add CMC FL5501~FL5505
By RF
0807 - SA
FL5501~5505 P/N Swap
by layout

SD_20201229
Remove CMC
FL5501、F5502、FF503、FL5504
Change to short pad
FR5501、ER5502、FR5503、FR5504、FR5505
FR5506、FR5507、FR5508、FR5509、FR5510.
Change to short pad

0602 -SA
delect touch

LCD POWER CIRCUIT

Layout 40 mil
3.3V (S0)
1st = 074.51711.009P
1.8V (S0)
Vgs(th) = 0.5~1.5V
1st = 075.00138.0A7C
2nd = 075.00138.0F7C
3rd = 075.00139.007C

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Display (LCD/Inverter)
Size: A2	Document Number: 13" CS ZURG Lucienne
Rev: -1	
Date: Wednesday, March 24, 2021	Sheet 55 of 106

TBD

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A01

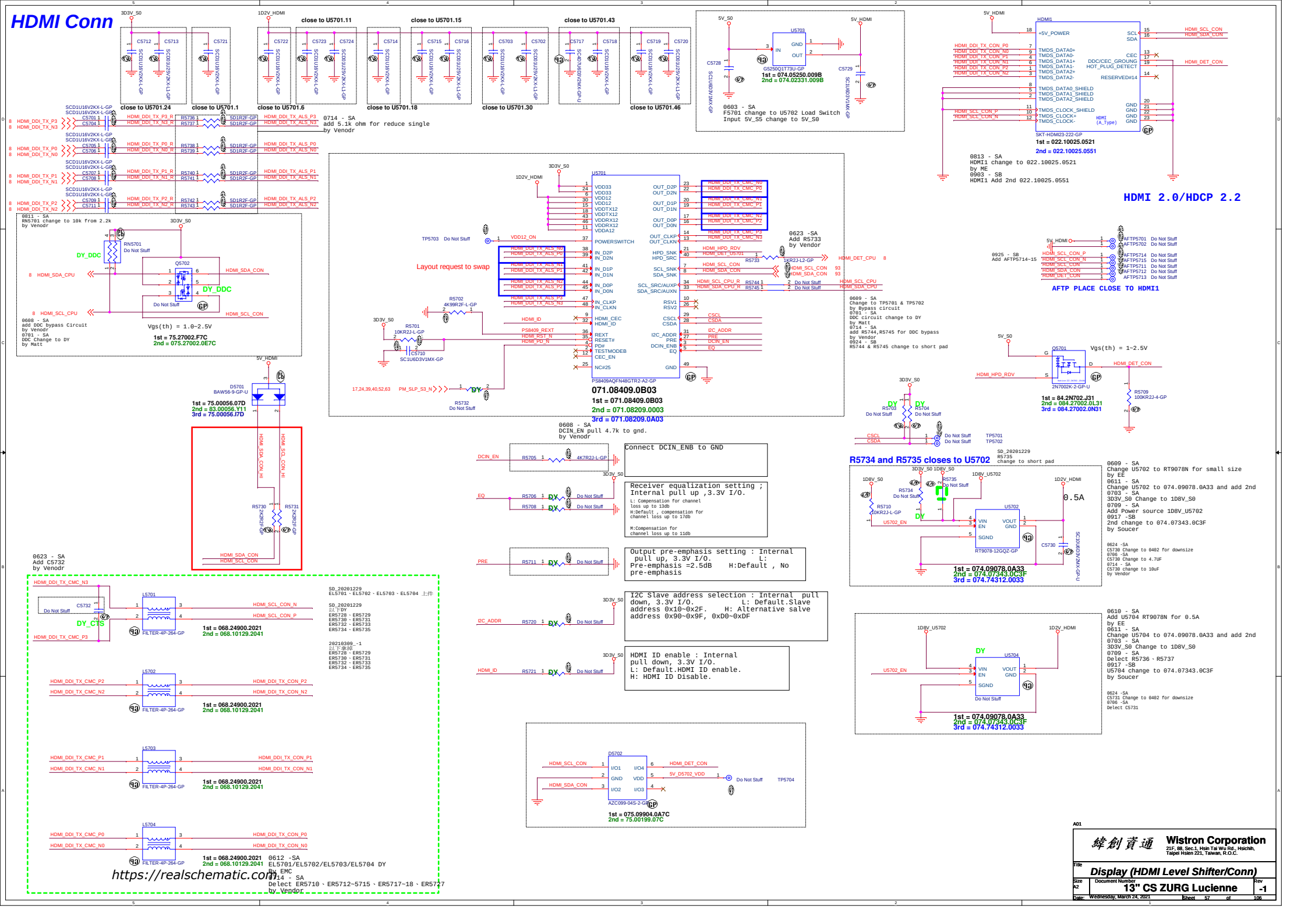
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (RSVD)*

Size	Document Number	Rev
A3	13" CS ZURG Lucienne	-1

Date: Wednesday, March 24, 2021 Sheet 56 of 106

HDMI Conn



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Title	Display (HDMI Level Shifter/Conn)
Size	A2
Document Number	13" CS ZURG Lucienne
Rev	-1
Date	Wednesday, March 24, 2021
Sheet	57 of 106

TBD

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A01

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Display (RSVD)***
Size A3	Document Number **'13" CS ZURG Lucienne**
Rev **-1**	
Date: Wednesday, March 24, 2021	Sheet 58 of 106

SSID = DVI

TBD

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A01

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (RSVD)*

Size	Document Number	Rev
A3	13" CS ZURG Lucienne	-1

Date: Wednesday, March 24, 2021 Sheet 59 of 106

SSID = SATA

SATA HDD Connector

TBD

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A01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

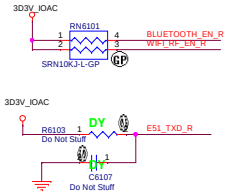
Title: INT IO (HDD/ODD)

Size: A4 | Document Number: 13" CS ZURG Lucienne | Rev: -1

Date: Wednesday, March 24, 2021 | Sheet 60 of 106

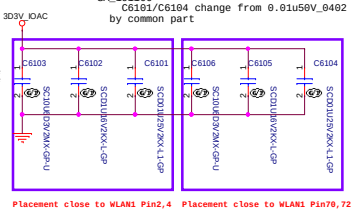
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

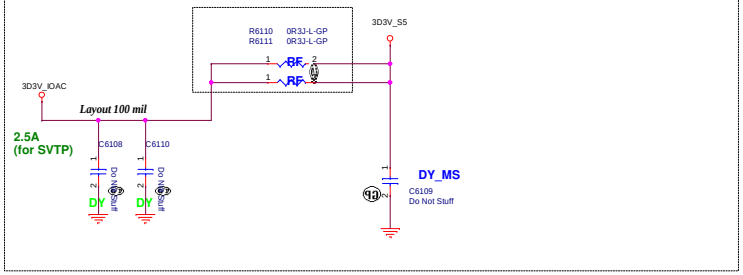


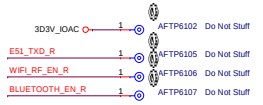
SA_191106
C6101/C6104 change from 0.01u50V_0402
by common part

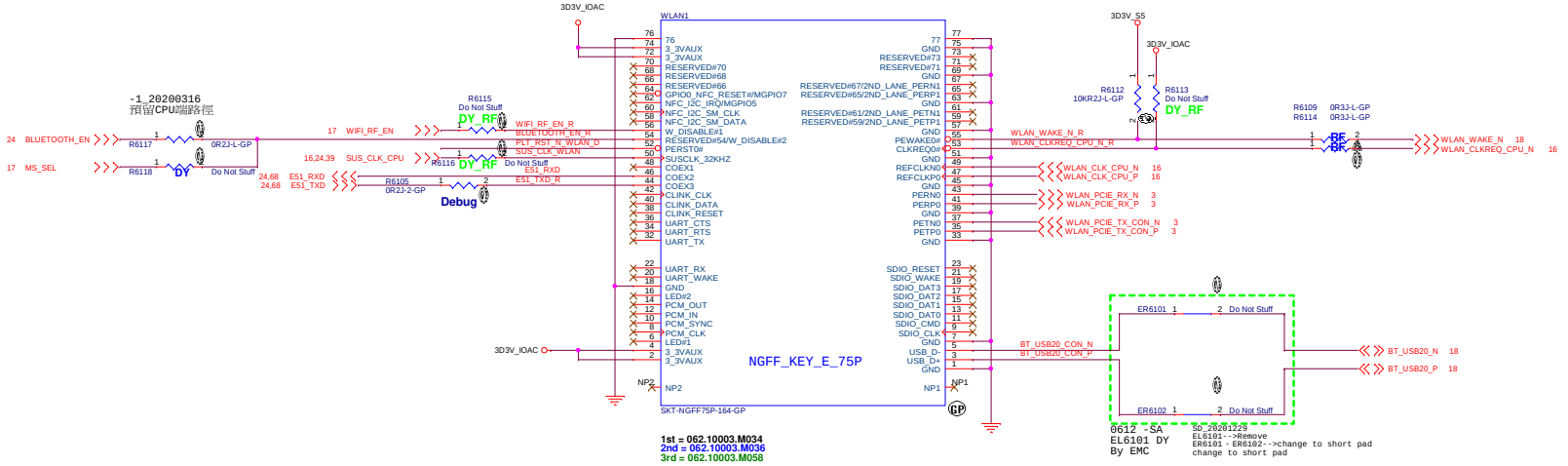
0624 -SA
C6103 Change to 0402 for downsize
C6106 Change to 0402 for downsize



Modern Standby CIRCUIT



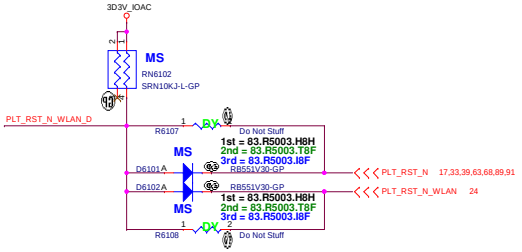




0612 -SA
EL6101 DY
By EMC

SD_20201229
EL6101-->Remove
ER6101、ER6102-->change to short pad
change to short pad

0903 -SB
WLAN1 1st change to 062.10003.M035
add 2nd 062.10003.M036
add 3rd 062.10003.M035
by CE
SC-20201111
3rd 062.10003.M035 change 062.10003.M058



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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	INT IO (WLAN M.2)	
Size A2	Document Number 13" CS ZURG Lucienne	Rev -1
Date: Wednesday, March 24, 2021	Sheet 61 of 106	

Shut down CIRCUIT

0727 -SA
Add Shut down circuit for power saving

SD_20201229
R6201
change to short pad

SD_20210308
R6201
short pad change to 0R

5V_LB_S5

LB
R6201
Do Not Stuff

5V_S5

Vgs(th) = 0.4~1.2

DY
C6219
Do Not Stuff

DY
R6202
Do Not Stuff

DY
C6220
Do Not Stuff

DY
Q6201
Do Not Stuff

1st = 084.03413.0031
2nd = 084.02301.0031
3rd = 84.00513.03B

DY
C6221
Do Not Stuff

DY
R6204
Do Not Stuff

LB_EN_N_R

17,24,39,40,63 PM_SLP_S5_N

Q6202
DY
LB_EN_N
Do Not Stuff

Vgs(th) = 1~2.5V

1st = 84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.27002.0N31

0624 -SA
C6202 Change to 0402 for downsize
Close to pin13

0624 -SA
C6205 Change to 0402 for downsize
Close to pin40

VSTBY33

0702 -SA
C6203 Change to 0201 for downsize
C6206 Change to 0201 for downsize

C6202 C6203 C6204 C6205 C6206 C6207
Do Not Stuff
LB

5V_LB_S5

Close to pin22、29

Close to pin14

0624 -SA
C6208 Change to 0402 for downsize
C6211 Change to 0402 for downsize
0702 -SA
C6209 Change to 0201 for downsize
C6212 Change to 0201 for downsize

C6208 C6209 C6210 C6211 C6212 C6213
Do Not Stuff
LB

0818-SA
Add R6210 & R6211
by EE

DY_LB
R6210 Do Not Stuff
R6211 Do Not Stuff
CPU_I2C3_SCL 17,93
CPU_I2C3_SDA 17,93

LB
R6208 Do Not Stuff
R6209 Do Not Stuff
LB_SCL 24
LB_SDA 24

U6201_SCL
U6201_SDA
U6201_GPC4
U6201_GPC5
TP6201
TP6202

0728 -SA
Add LB_SCL & LB_SDA net
by EE

5V_LB_S5

U6201

VSTBY33 13 VSTBY33
40 VSTBY33
22 VLED5
29 VLED5
14 VIN5
VCOREB 12 VCOREB
VCOREB2 9 VCOREB2
LEDCS0 35 LEDCS0/PWM0/SMISO0/GCLK0/GPA0
LEDCS1 30 LEDCS4/PWM4/SMISO1/GPA4
LEDCS2 15 LEDCS5/PWM5/SSCK1/GPA5
LEDCS3 20 LEDCS8/GSW0/PWM8/GPB0
LEDCS4 21 LEDCS9/GSW1/PWM9/GPB1
LEDCS5 28 LEDCS10/GSW2/PWM10/GPB2
27 LEDCS11/GSW3/PWM11/GPB3
25 LEDCS12/GSW4/PWM12/GPB4
24 LEDCS13/GSW5/PWM13/GPB5
GPB6 23 GSW6/PWM14/GPB6
18 LB_USB20_P 39 DP
18 LB_USB20_N 38 DM
U6201_WRST_N 3 WRST#

SMCLK0/GPC0 4
SMDAT0/GPC1 5
SMCLK1/GPC2 6
SMDAT1/GPC3 7
TXD/GPC4 2
RXD/GPC5 1
STRIP1/PSW0/TACH2D/GPC6 10

LEDCOM0/PSW0/TACH0A/SSCK0/GPG0 36 LEDCOM0
LEDCOM1/PSW1/SMISO1/TACH1A/GPG1 34 LEDCOM1
LEDCOM2/PSW2/SSCE1#/TACH2A/GPG2 33 LEDCOM2
LEDCOM3/PSW3/SMOSI1/TACH0B/GPG3 32
LEDCOM4/PSW4/SSCK1/TACH1B/GPG4 31
LEDCOM5/PSW5/TACH2B/SMOSI0/GPG5 16
LEDCOM6/PSW6/GCLK0/SMISO0/TACH0C/GPG6 17
LEDCOM7/PSW7/SSCE0#/TACH1C/GPG7 18

PSW8/SMOSI0/TACH2C/GPH0 19
STRIP0/PSW1/TACH1D/GPH2 11

VSS 8
VSS 26
VSS 37
THERMAL_PAD 41

Do Not Stuff
1st = 071.08233.M002

0713 -SA
Rename LEDCS0~2 and add LEDCS3~5
by ite

0713 -SA
Remove LEDCOM3~5
by ite

0813 -SA
U6201 change to 071.08233.M002 for empty FW
by EE

5V_LB_S5
D6201 Do Not Stuff
R6203 Do Not Stuff
1st = 83.R2003.A8M
2nd = 083.52030.008F
LB LB
C6218
Do Not Stuff
LB

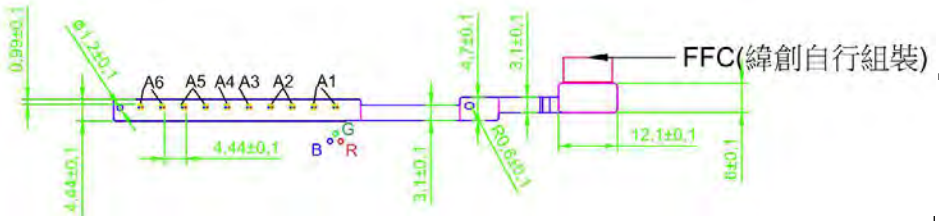
0702 -SA
C6218 Change to 0201 for downsize

0624 -SA
C6214 Change to 0402 for downsize
Close to pin12

VCOREB
C6214 C6215
Do Not Stuff
LB

0624 -SA
C6216 Change to 0402 for downsize
Close to pin9

VCOREB2
C6216 C6217
Do Not Stuff
LB



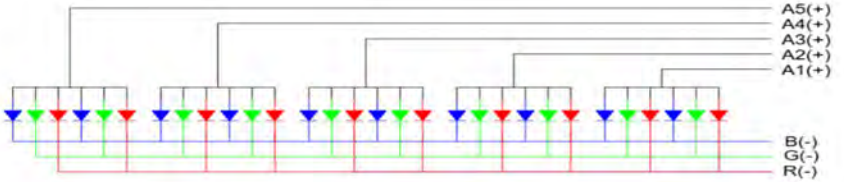
Do Not Stuff
LB1
LB
1st = 020.K0175.0010
2nd = 20.K0642.010
3rd = 020.K0376.0010

LEDCOM0
LEDCOM1
LEDCOM2
LEDCS0
LEDCS1
LEDCS2
LEDCS3
LEDCS4
LEDCS5

3D3V_S5
R6205 Do Not Stuff
DY
GPB6
R6206 Do Not Stuff
DY

From: Ian.Lin@ite.com.tw <Ian.Lin@ite.com.tw>
Sent: Thursday, July 23, 2020 11:13 AM
To: Marvin Chen/WHQ/Wistron <Marvin_Chen@wistron.com>; Eugene Chen/WHQ/Wistron <E
Cc: Jack CH Yu/WHQ/Wistron <Jack_CH_Yu@wistron.com>; Norman Hung/WHQ/Wistron <Nor
<Willy_Hsu@wistron.com>; James CS Lin/WHQ/Wistron <James_CS_Lin@wistron.com>; Charle
Mitch.Huang@ite.com.tw; migi.lee@ite.com.tw
Subject: RE: Wistron_ZURG_13"_Light Bar_Circuit double confirm_20200622

Dear Marvin:
補充 Q1: SMBus slave address:0xAA.
謝謝.



Pin Definition									
Pin1	Pin2	Pin3	Pin4	Pin5	Pin6	Pin7	Pin8	Pin9	Pin10
R	G	B	A1	A2	A3	A4	A5	A6	None
-	-	-	+	+	+	+	+	+	None

SD_20201225 Swap Pin
SD_20201230 換料號020.K0175.0010
SD_20200104 新增20.K0642.010
SD_20200104 新增020.K0376.0010

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A01

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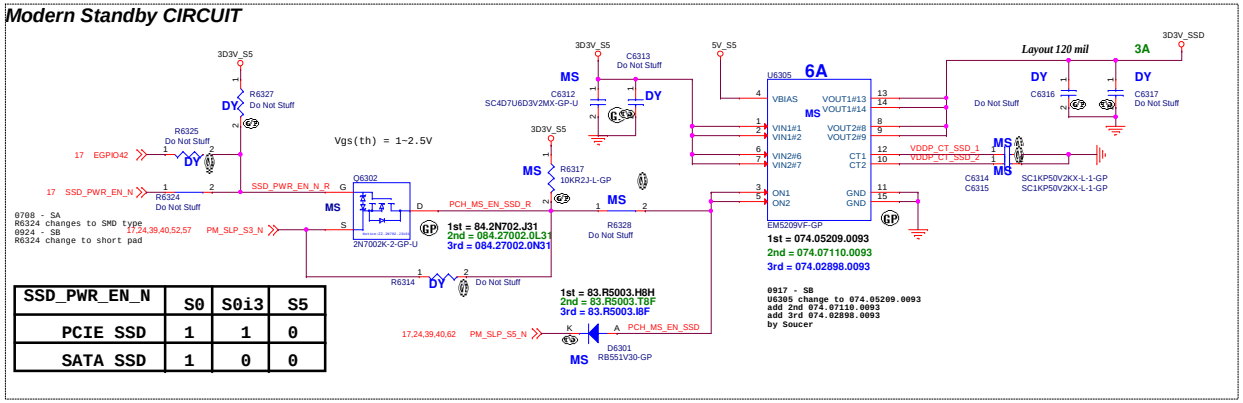
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Light Bar**
Size: A3
Document Number: 13" CS ZURG Lucienne
Rev: -1
Date: Wednesday, March 24, 2021
Sheet 62 of 106

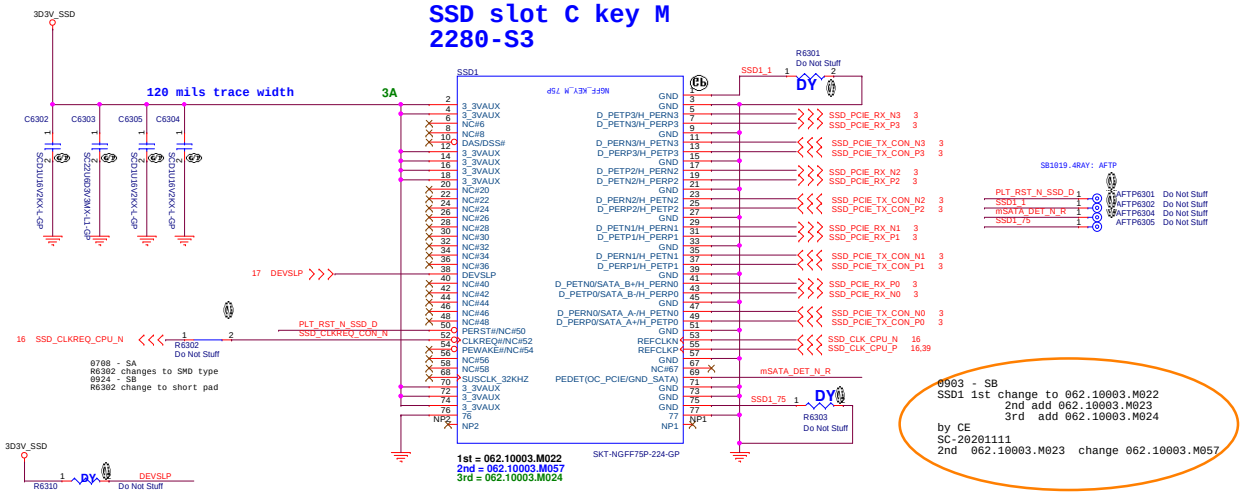
NGFF Connector

Modern Standby CIRCUIT



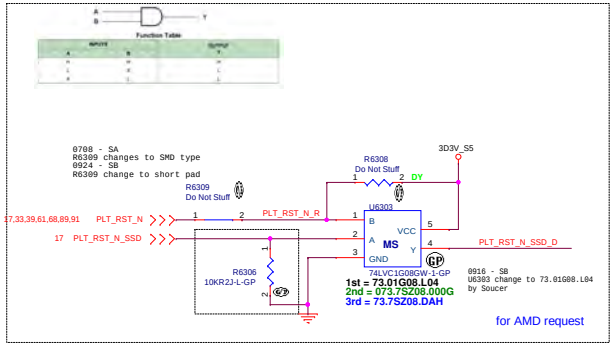
SSD_PWR_EN_N	S0	S0i3	S5
PCIE SSD	1	1	0
SATA SSD	1	0	0

SSD slot C key M 2280-S3

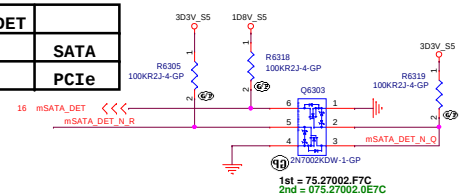


0903 - SB
SSD1 1st change to 062.10003.M022
2nd add 062.10003.M023
3rd add 062.10003.M024
by CE
SC-20201111
2nd 062.10003.M023 change 062.10003.M057

0721 - SA
Remove ED6303~ED6304 for layout



mSATA_DET	
0	SATA
1	PCIe



5.3. SSD Socket; Socket 3 (Mechanical Key M)

This Socket pinout and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to four lanes or SATA. The state of the PEDET pin (69) will indicate to the platform which I/F of these two is actually connected.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

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A01		
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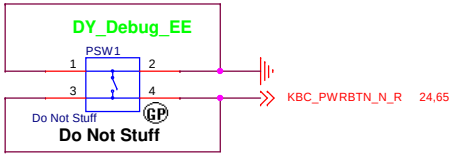
Title: INT IO (SSD M.2)		
Size: A2	Document Number: 13" CS ZURG Lucienne	Rev: -1
Date: Wednesday, March 24, 2021	Sheet 63 of 106	

Power Button



Vol_up/down BTN

Privacy Cam

0602 - SA
Delect Pricacy circuit

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A01

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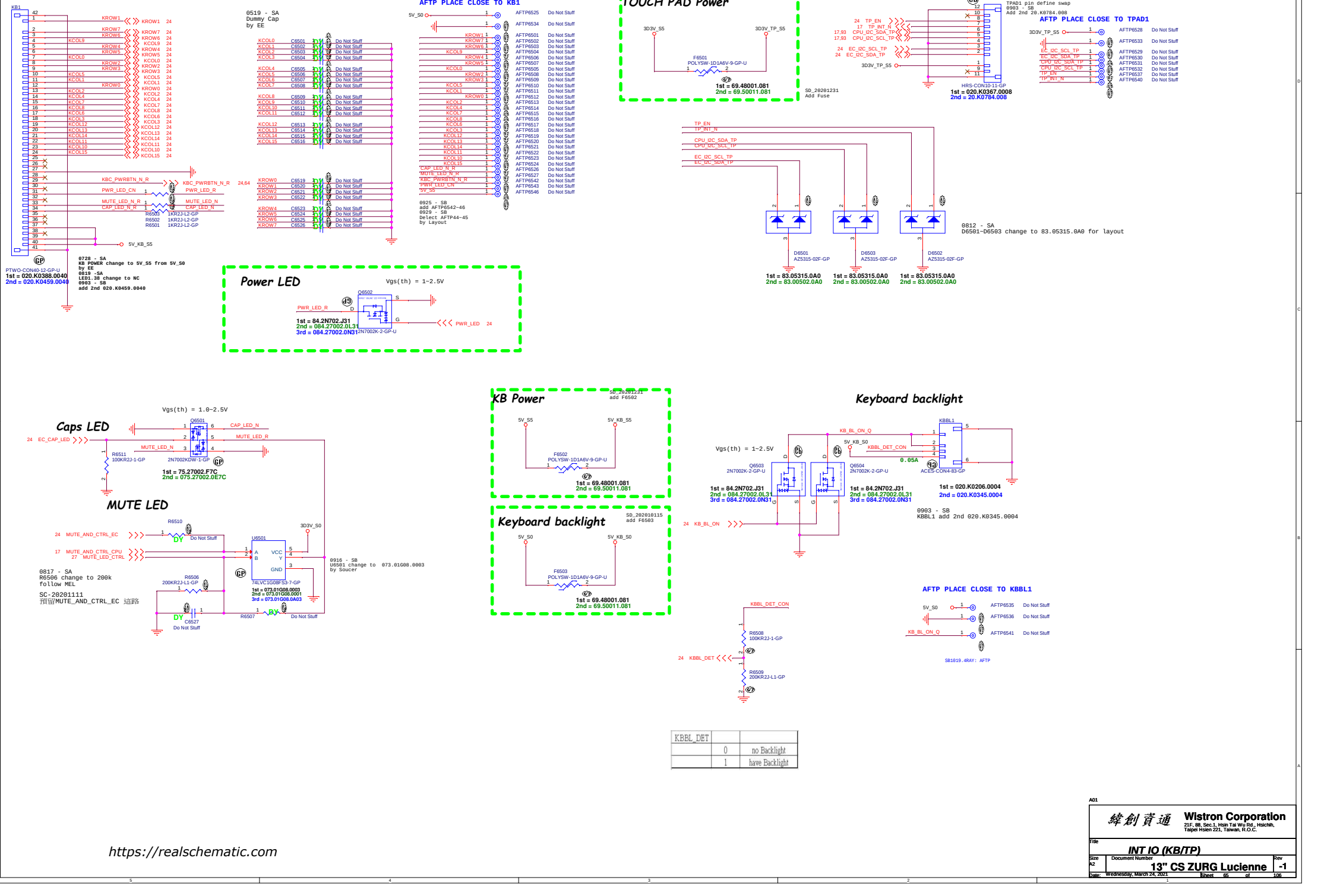
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***LED / Button / Power Button***	
Size A3	Document Number **13" CS ZURG Lucienne**	Rev **-1**
Date: Wednesday, March 24, 2021	Sheet 64 of 106	

SSID = Key Board CN & TP CN



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Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	INT IO (KB/TP)
Size: A2	Document Number: 13" CS ZURG Lucienne
Rev	-1
Date: Wednesday, March 24, 2021	Sheet 65 of 106

IO Board Connector

0602 -SA
Delect IO1 connector
by EE

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A01

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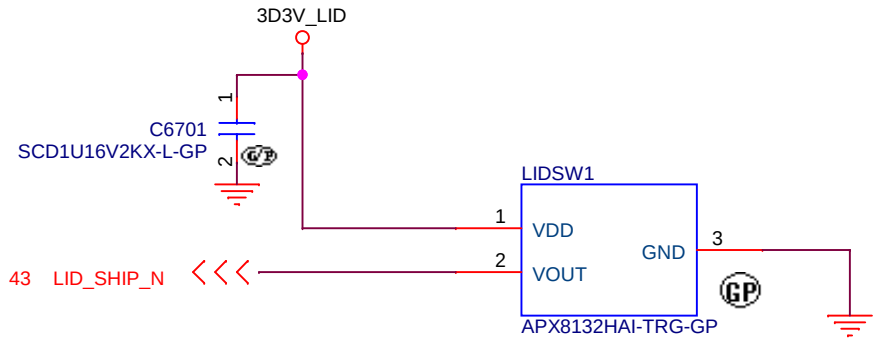
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RSVD

Size	Document Number	Rev
A4	13" CS ZURG Lucienne	-1

Date: Wednesday, March 24, 2021 Sheet 66 of 106

SSID = Hall sensor



Pin2:Out Push-Pull Type

0923 - SB
LIDSW1 change to 074.08132.0A7B
by ME

0603 - SA
Remove LIDSW1 and move to IO2

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A01

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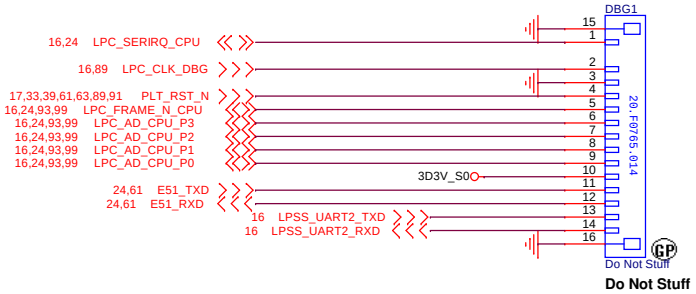
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Sensor (Hall-Sensor)***	
Size A	Document Number **13" CS ZURG Lucienne**	Rev **-1**
Date: Wednesday, March 24, 2021	Sheet 67 of 106	

Debug CONN



Do Not Stuff

Debug CONN (for AMD LPC interface debug)

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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug (LPC debug)***

Size: A3 | Document Number: **13" CS ZURG Lucienne** | Rev: -1

Date: Wednesday, March 24, 2021 | Sheet 68 of 106

SENSOR HUB
AMD ONLY

TBD

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A01

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Sensor (GYROSCOPE/PRESSUE/ALS)

Size	Document Number	Rev
A3	13" CS ZURG Lucienne	-1

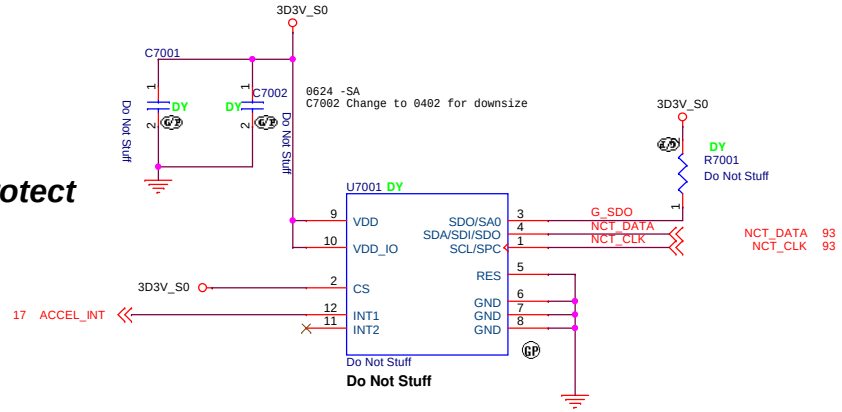
Date: Wednesday, March 24, 2021 Sheet 69 of 106

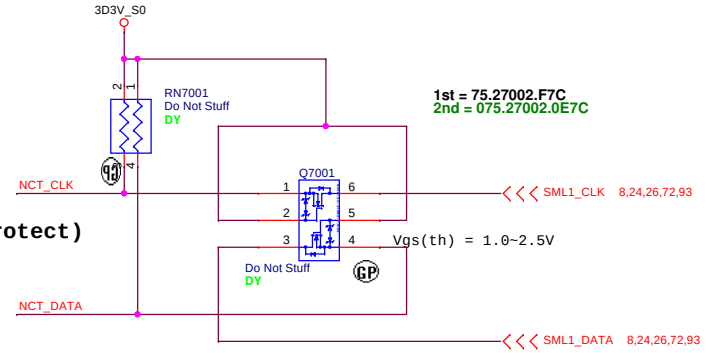
G-sensor

Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

To KBC
for HDD Protect





G-sensor(HDD Protect)

Must be placed in the center of the system

SC-20201113
DY R7001、U7001、C7001、U7002、RN7001、Q7001

To Sensor HUB
for LCD angle

0602 -SA
Delect U7002

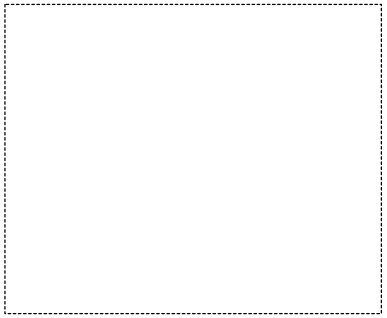


Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (G-sensor)***

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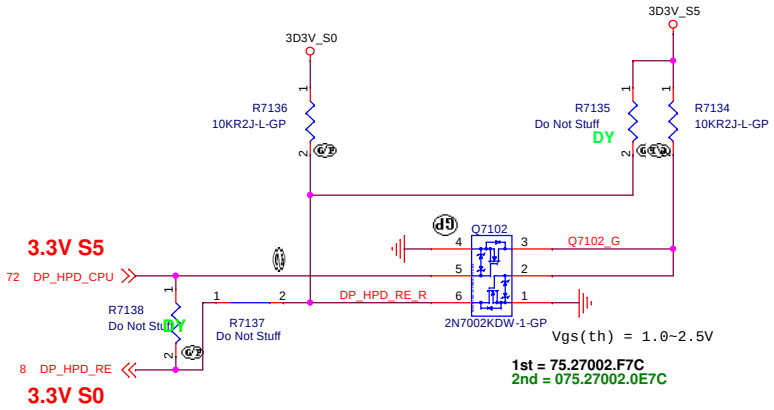
Mux Redriver For Type C



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A01

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Title: **EXT IO (Thunderbolt(1/3)/Type C Re-driver)**

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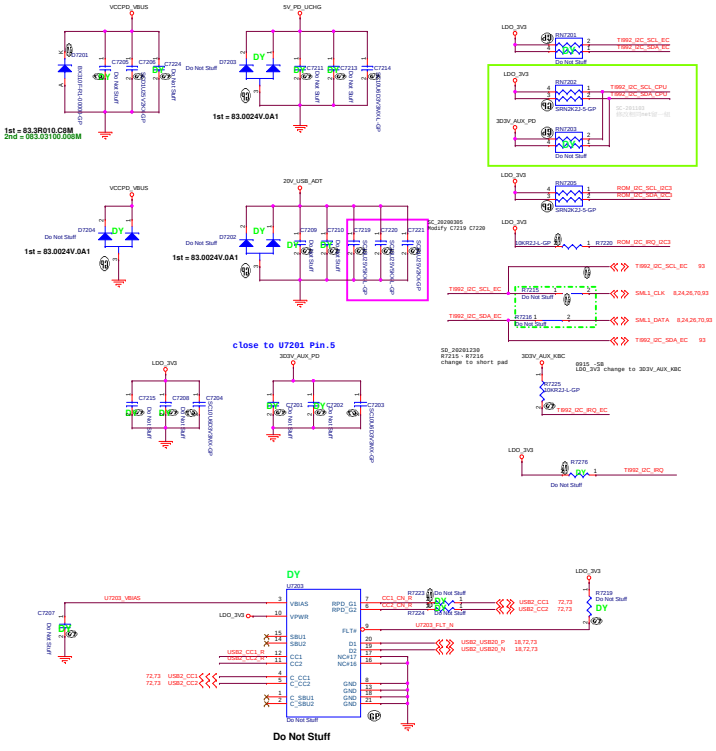
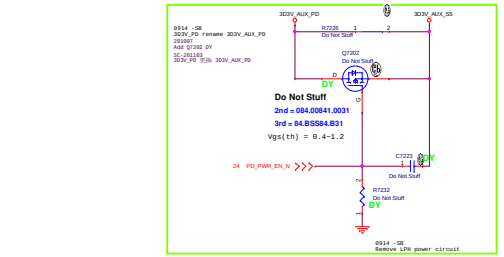
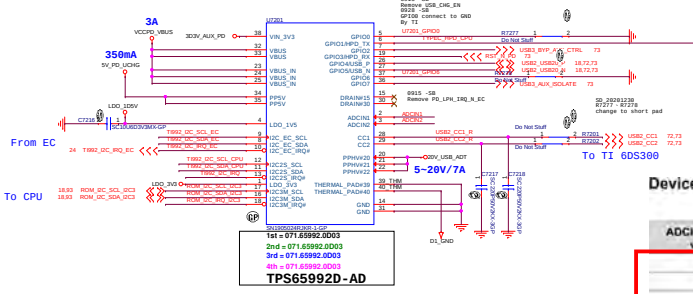
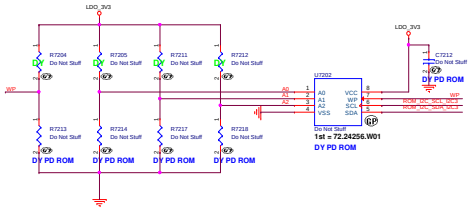
TI TPS65992D









Device Functional Modes (continued)

Table 6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value (1)	ADCIN2 decoded value (1)	I²C address index (2)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
5	7	#4	
7	3	#1	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the 'APP' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable he sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode.
6	0	#3	
5	7	#4	

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DiV = R_{DOWN} / (R_{UP} + R_{DOWN}) (1)			Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
0.9061	0.9530	1.0	tie to LDO_3V3	7

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緯創資通	Wistron Corporation	
Title: EXT IO (Thunderbolt(1/3)/Type C CC Logic)		
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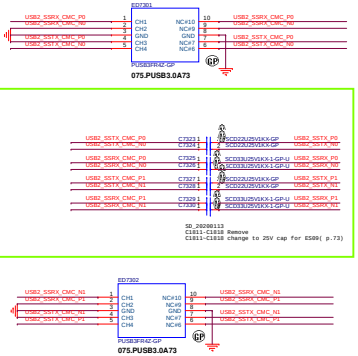
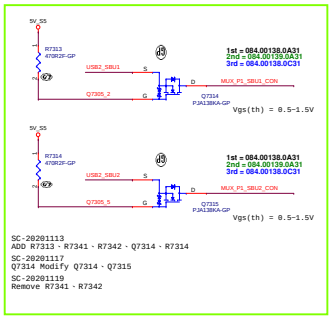
USB Type C Connector

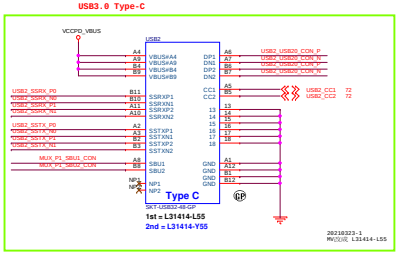
OUTPUT=3A

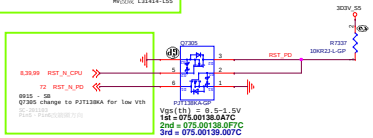


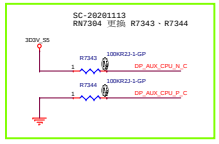


Gen2/DP1.4(HBR3)/PD3.0

USB3.0 Type-C







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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***EXT IO (RSVD)***

Size	Document Number	Rev
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A01

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
EXT IO (RSVD)

Size	Document Number	Rev
A3	**13" CS ZURG Lucienne**	**-1**

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Title: **GPU (RSVD)**		
Size	Project Name: **Pacific Ocean 15"**	Rev: MV
Date: Wednesday, March 24, 2021	Sheet 76 of 106	

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Title: **GPU (RSVD)**		
Size	Project Name: **Pacific Ocean 15"**	Rev: **MV**
Date: Wednesday, March 24, 2021	Sheet 77 of 106	

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Title: GPU (RSVD)		
Size	Project Name: Pacific Ocean 15"	Rev: MV
Date: Wednesday, March 24, 2021	Sheet 78 of 106	

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Title	GPU (RSVD)	
Size	Project Name: Pacific Ocean 15"	Rev: MV
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Title: **GPU (RSVD)**		
Size	Project Name: **Pacific Ocean 15"**	Rev: **MV**
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Title	***GPU (RSVD)***	
Size: A4	Document Number: **13" CS ZURG Lucienne**	Rev: **-1**
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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

Size	Document Number	Rev
A4	**13" CS ZURG Lucienne**	-1

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

Size: A3 | Document Number: **13" CS ZURG Lucienne** | Rev: **-1**

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Title	***UNUSED PARTS (RSVD)***	
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ME

Screw pad

0819 -SA
H3 - H7 change to ZZ.00PAD.6U1
by ME

0611 -SA
Add H11~H14
by ME

0611 -SA
Delect H4
by ME

Screw nut

Clip

0611 -SA
Delect CL1~CL10& CL17 - CL18

Add moe CAP for Acoustic

0615 -SA
C0927 change to mount
by EE
0908 -SB
C0927 change to 077.53361.0021

0908 -SB
C0928 change to 077.53361.0021

0902 - SB
C0929 change to DY
0908 -SB
C0929 change to 077.53361.0021
0615 -SA
C0930 change to mount
by EE
0902 - SB
C0930 change to DY
0908 -SB
C0930 change to 077.53361.0021

SC-20201119
Add 2nd 077.23361.0001
3rd 077.53361.0031
4th 79.33612.20L

EMI

0615 -SA
Delect SPR2,SPR3 and SPR4
By EMC
0714 - SA
Delect SPR1
by EMC

0602 -SA
Delect CPU_I2C_SCL_SENSOR &
CPU_I2C_SDA_SENSOR &
Touch circuit

close to DM2
close to DM1
close to CPU1
close to PU4403
close to PU4405
close to PQ4701
close to PQ4702
close to PQ4801
close to HDMI1
close to PU4403
close to PU5104
close to PU4404
close to PU4501
close to PU4551
close to PU4701
close to PU4703
close to PU4801
close to LCD1
close to CAM1

0728 - SA
Add EC8923-30
by EMC DK

0922 - SB
EC8925 mount
by EMC

0922 - SB
EC8926 mount
by EMC

0922 - SB
EC8927 mount
by EMC

0731 - SA
EC8928 Change to 0603 for Common part
by EE

RF

close to SO-DIMM
close to CPU
close to C1130
close to EC
close to U2701
close to DCIN1
close to RT2602
close to USB1
close to LCD1
close to SSD1
close to DDR4-CHA
close to U7201
close to USB3
close to LCD1
close to U7201
close to SO-DIMM
close to CPU
close to U7201
close to LCD1
close to U7201

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Title: UNUSED PARTS (RF/EMI Capacitors)
Size: A1
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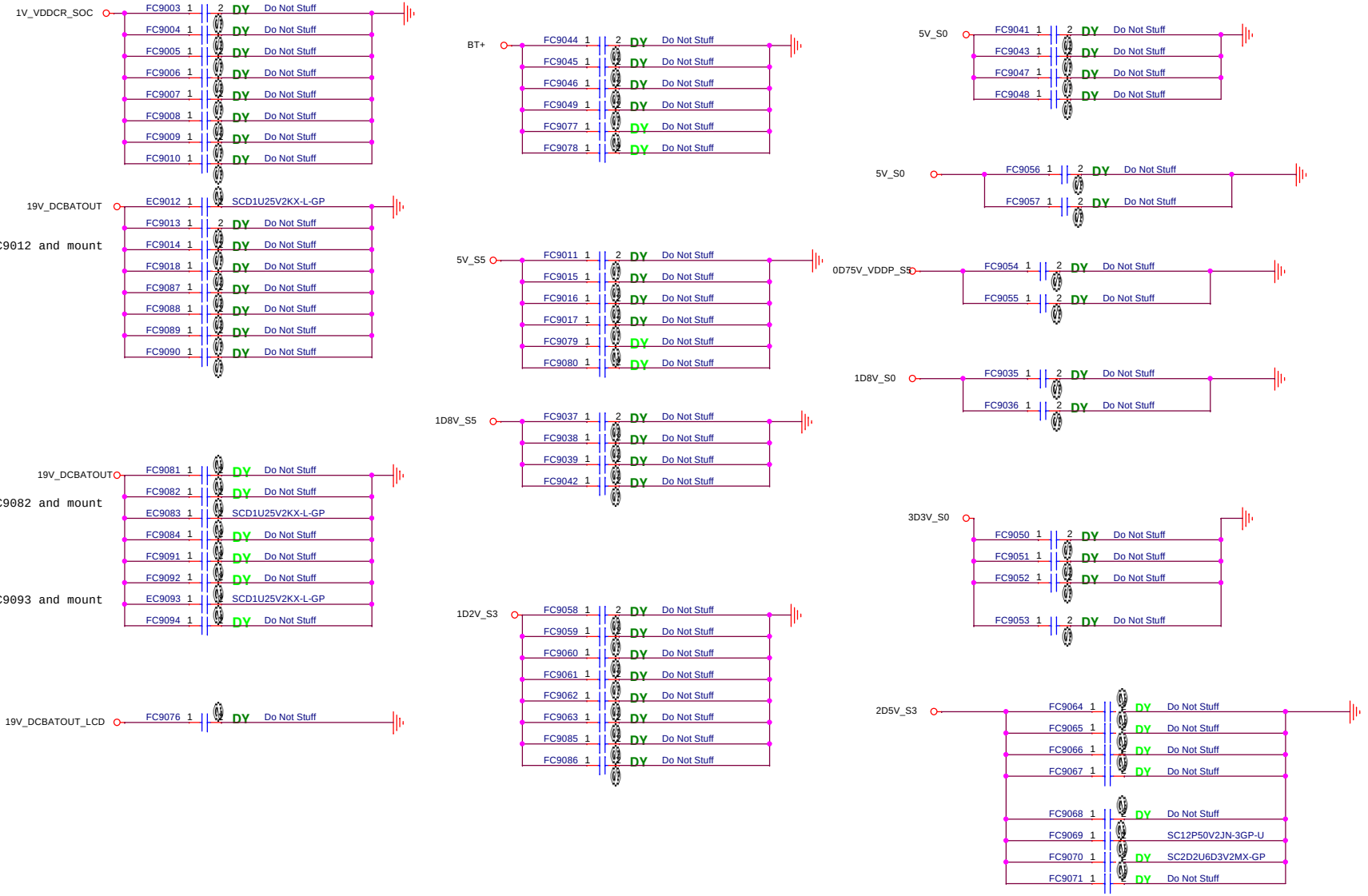
RF



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Title: ***INT IO (RSVD)***

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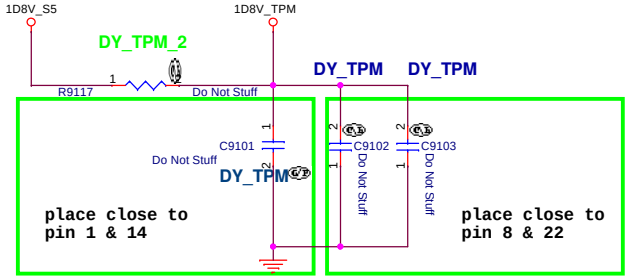
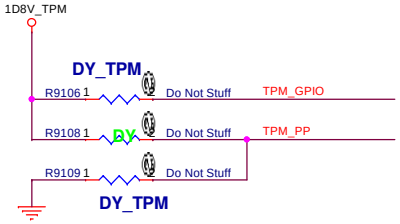
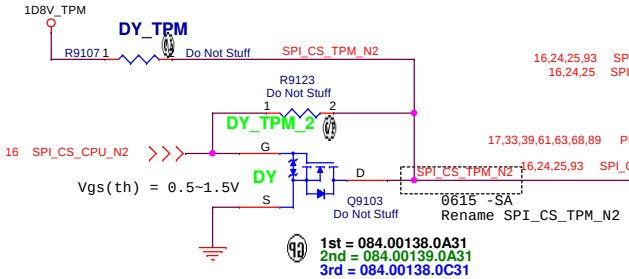
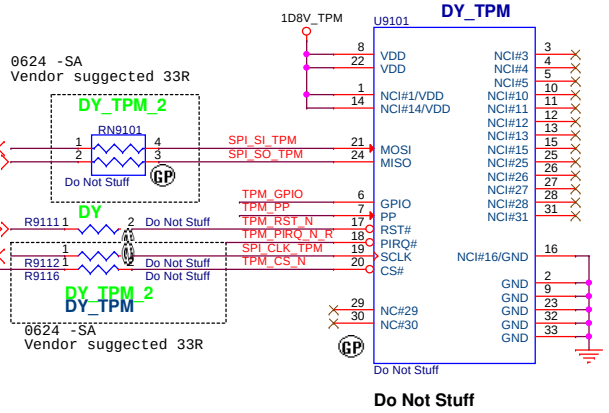
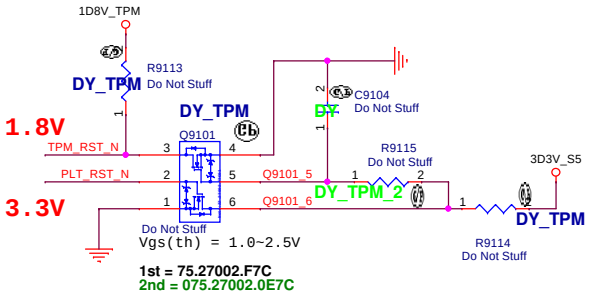


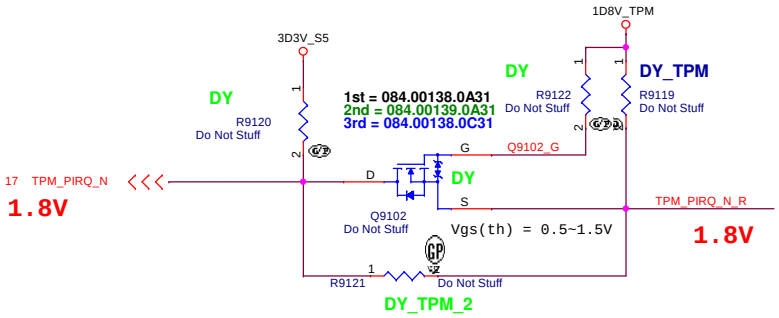






Do Not Stuff





93 SPI_CLK_TPM — SPI_CLK_TPM
93 SPI_SI_TPM — SPI_SI_TPM
93 SPI_CS_TPM_N2 — SPI_CS_TPM_N2
0615 -SA
Rename SPI_CS_TPM_N2

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Title: ***INT IO (TPM)***

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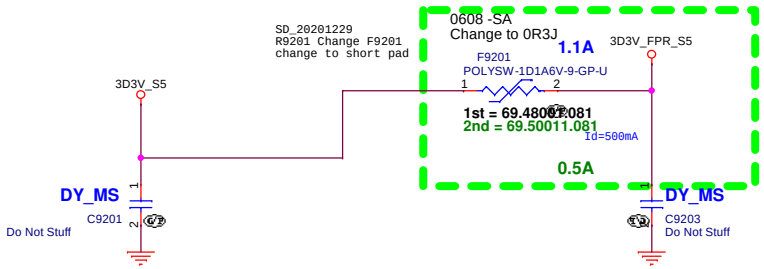
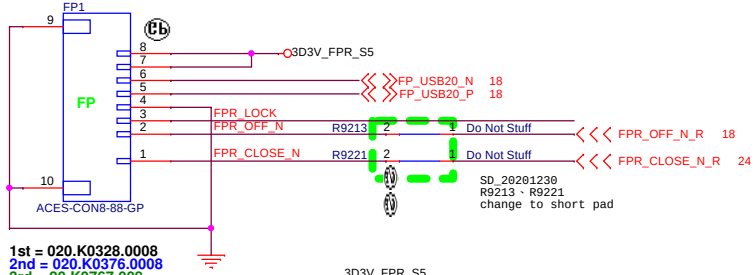
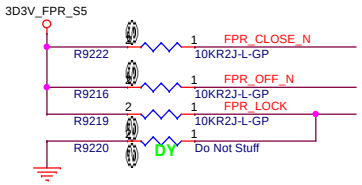
SSID = Finger Printer

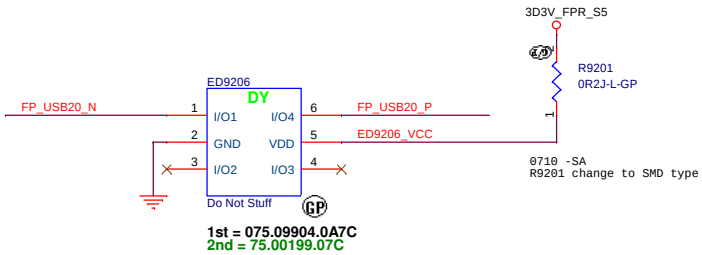
Modern Standby CIRCUIT





0903 - SB
FP1 add 2nd 020.K0376.0008
3rd 20.K0767.008



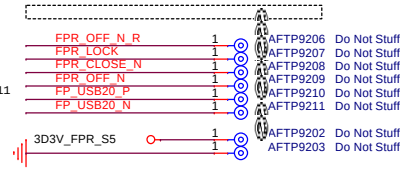


0710 -SA
R9201 change to SMD type

3.3V

0602 - SA
Delect PRIVACY_CAM_SW &
AFTP9204

0925 - SB
Add AFTP9208~11



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Title: INT IO (Finger printer)

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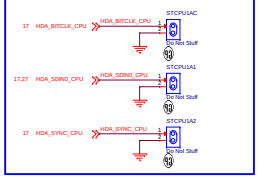
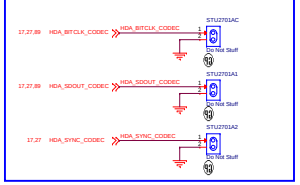
SITP DSN Template for ZURG_RENOIR

0707 -SA
SITP change to ZZ.PAD01.XN1
0806 -SA
SITP change to ZZ.PAD01.XL1

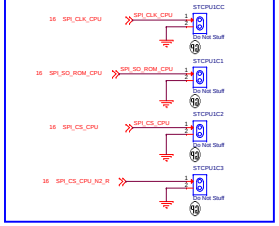
HDA SITP Priority 1
Close CPU1(p.17)



HDA SITP Priority 1
Close U2701(p.27)

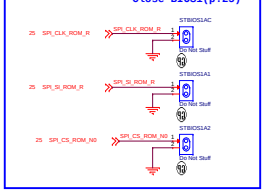


SPI SITP Priority 3
Close CPU1(p.16)



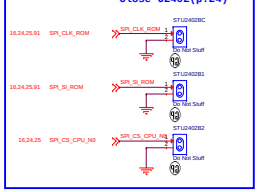
0922 -SB
STU7201AC - STU7201A1 - STU7201A2 are removed

SPI SITP Priority 3
Close BIOS1(p.25)



0922 -SB
STU7202AC - STU7202A1 - STU7202A2 are removed

SPI SITP Priority 3
Close U2402(p.24)



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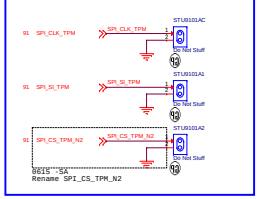

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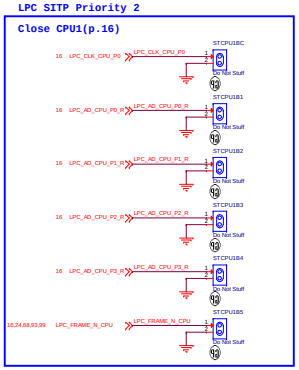

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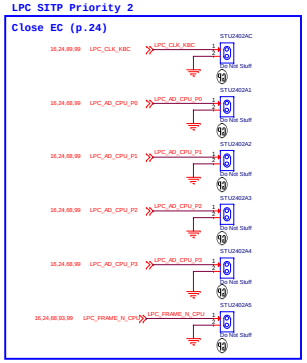

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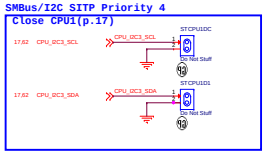

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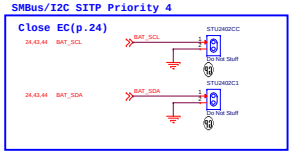

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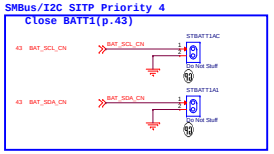

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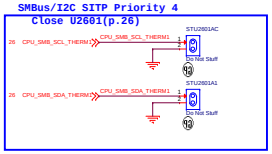

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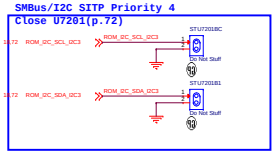

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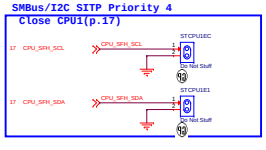

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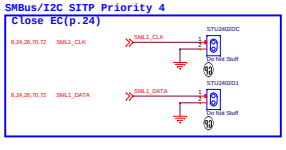

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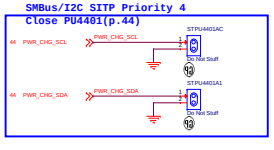

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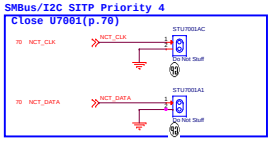

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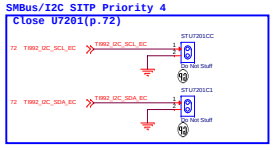

0817 -SA
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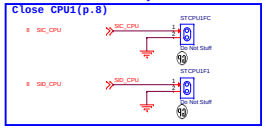

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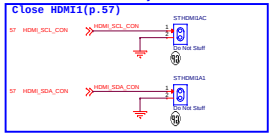

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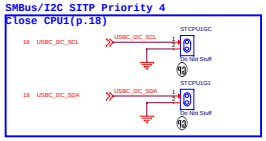

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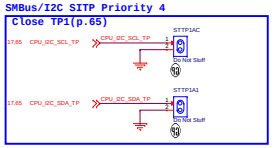

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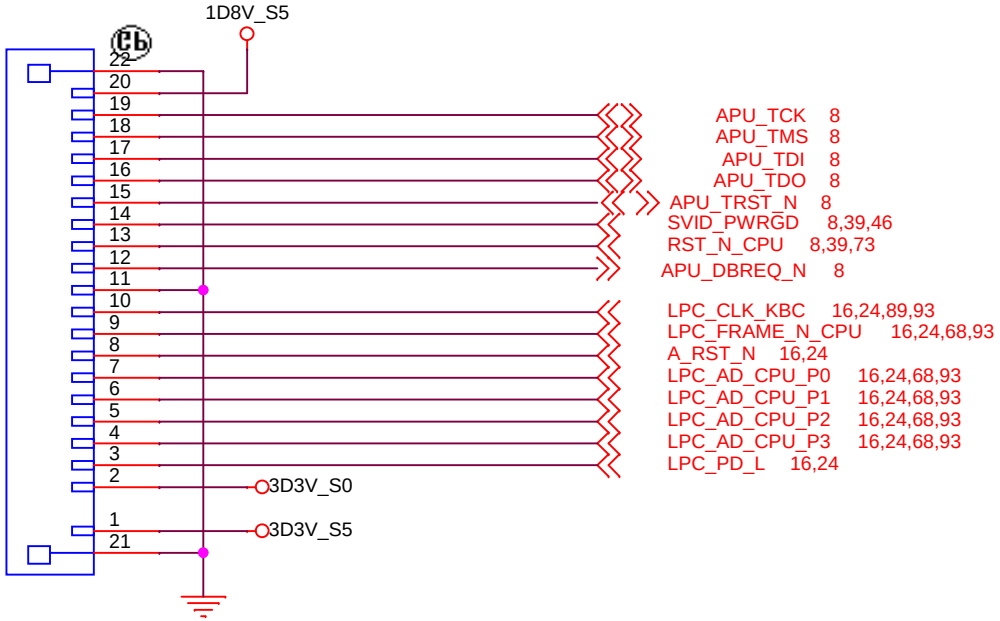

HDT1
Do Not Stuff

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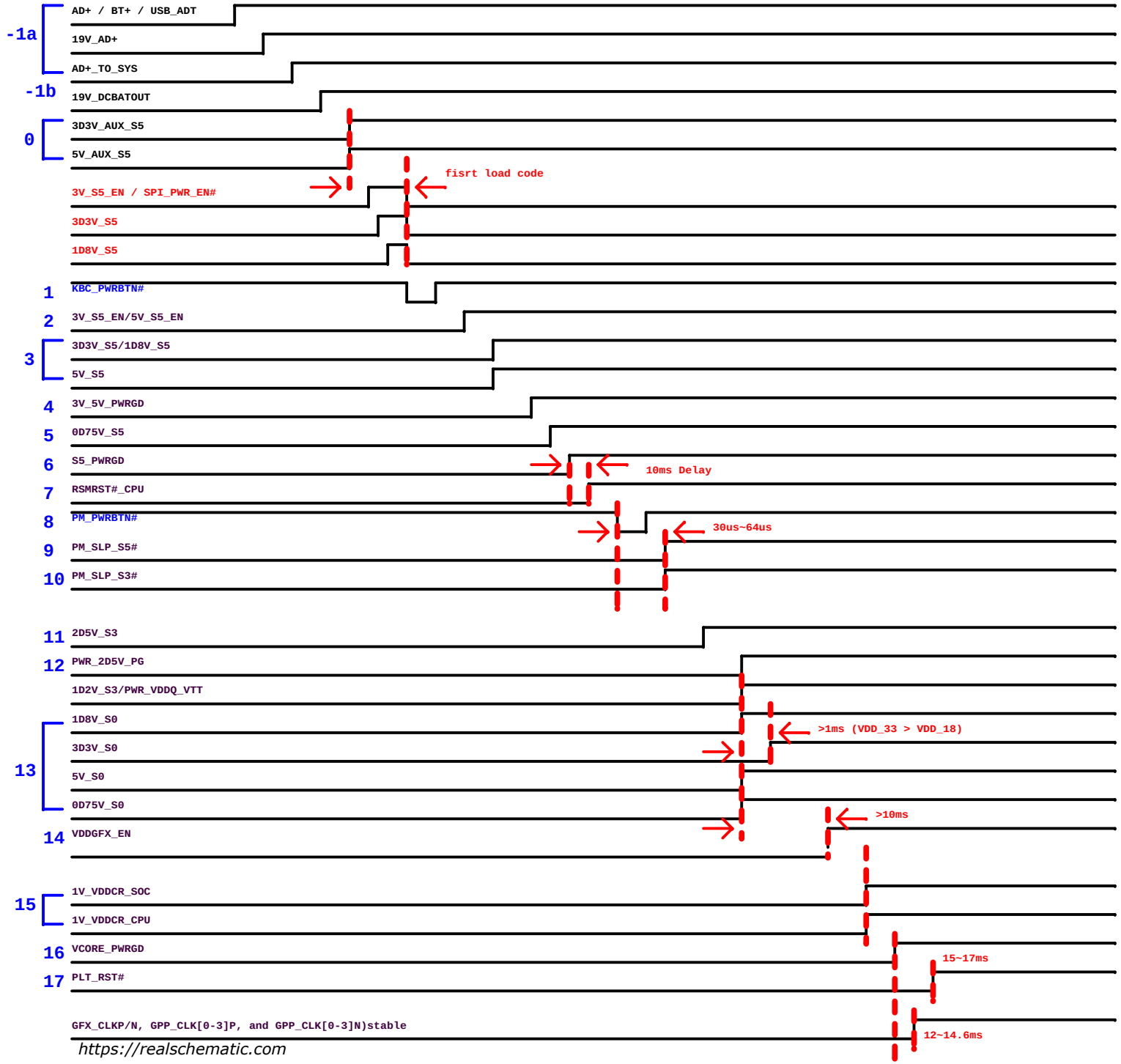
Non-Modify



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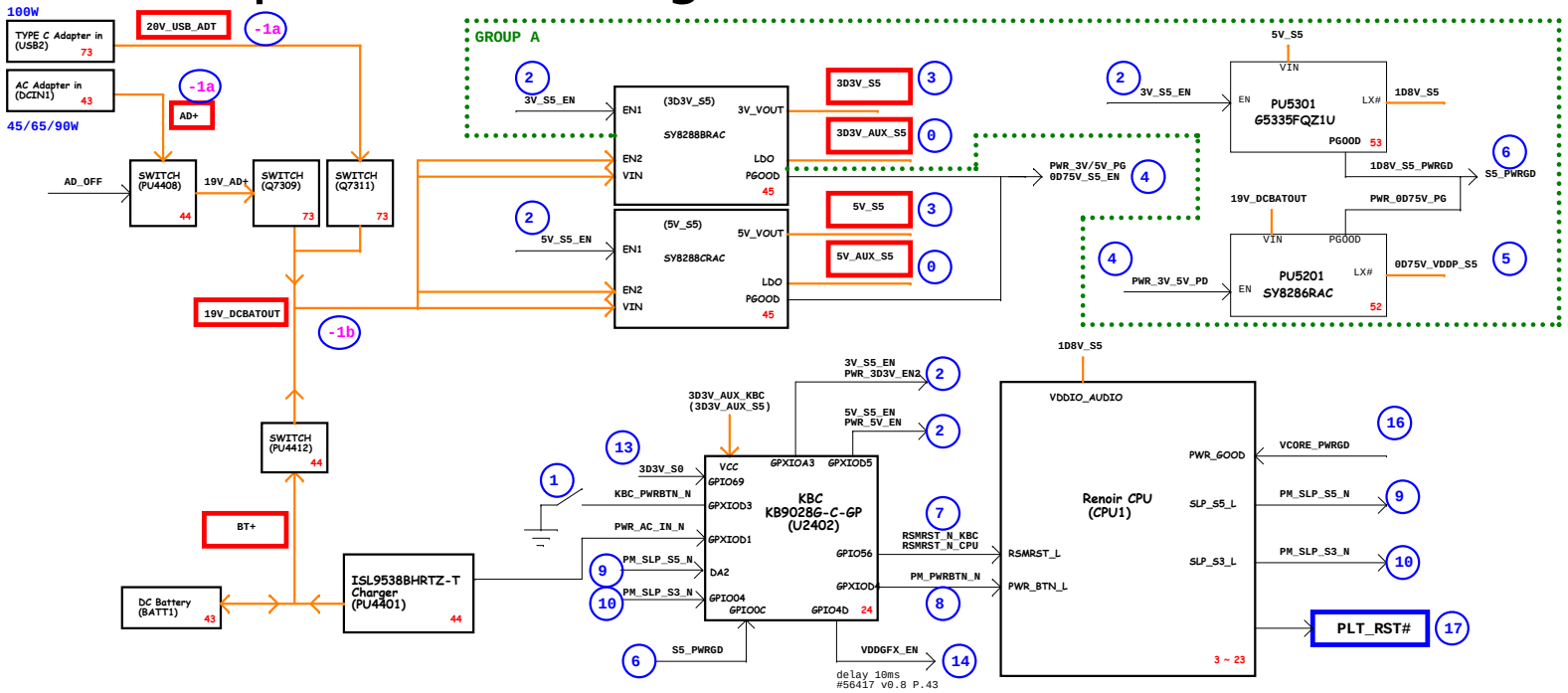
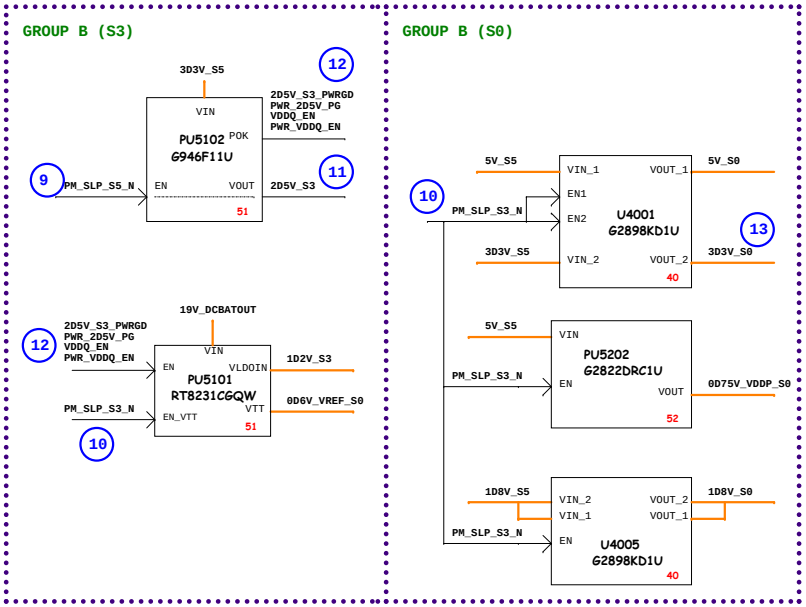
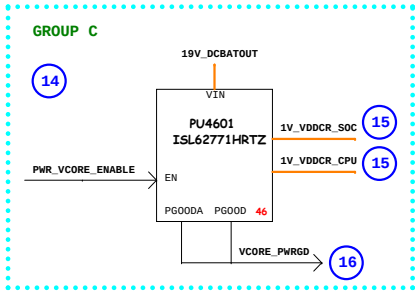
Power Sequence Block Diagram







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#56417 v0.8

Table 40. Power Sequencing Group Definitions without coin cell battery

Group	System Power Domain	Voltages
Group A	G3/S5	VDDBT_RTC_G, VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5
Group B	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP: (Add delay (>1ms) between VDD_33 and VDD_18 ramp up power sequence).
Group C	S0	VDDCR_SOC, VDDCR_CPU** (AM4 only), VDDCR* (FP6 only)

#56417 v0.8

17.1.2 Power-Up Power Sequencing Group Requirements

- All power supplies in Power Sequencing Group A must be stable and within specification before any power supply in Power Sequencing Group B is greater than 10 percent of its specified typical operating value.
- All power supplies in Power Sequencing Group B must be stable and within specification before any power supply in Power Sequencing Group C is greater than 10 percent of its specified typical operating value..
- If using group definitions from Table 41 on page 42, all power supplies in Power Sequencing Group C must be stable and within specification before any power supply in Power Sequencing Group D is greater than 10 percent of its specified typical operating value.
- All power supplies in Power Sequencing Group C (if using Table 40 on page 42) or Power Sequencing Group D (Table 41 on page 42) must be stable and within specification one ms before the assertion of PWR_GOOD.
- Firmware control is required to control the operating voltage of VDDCR_SOC.

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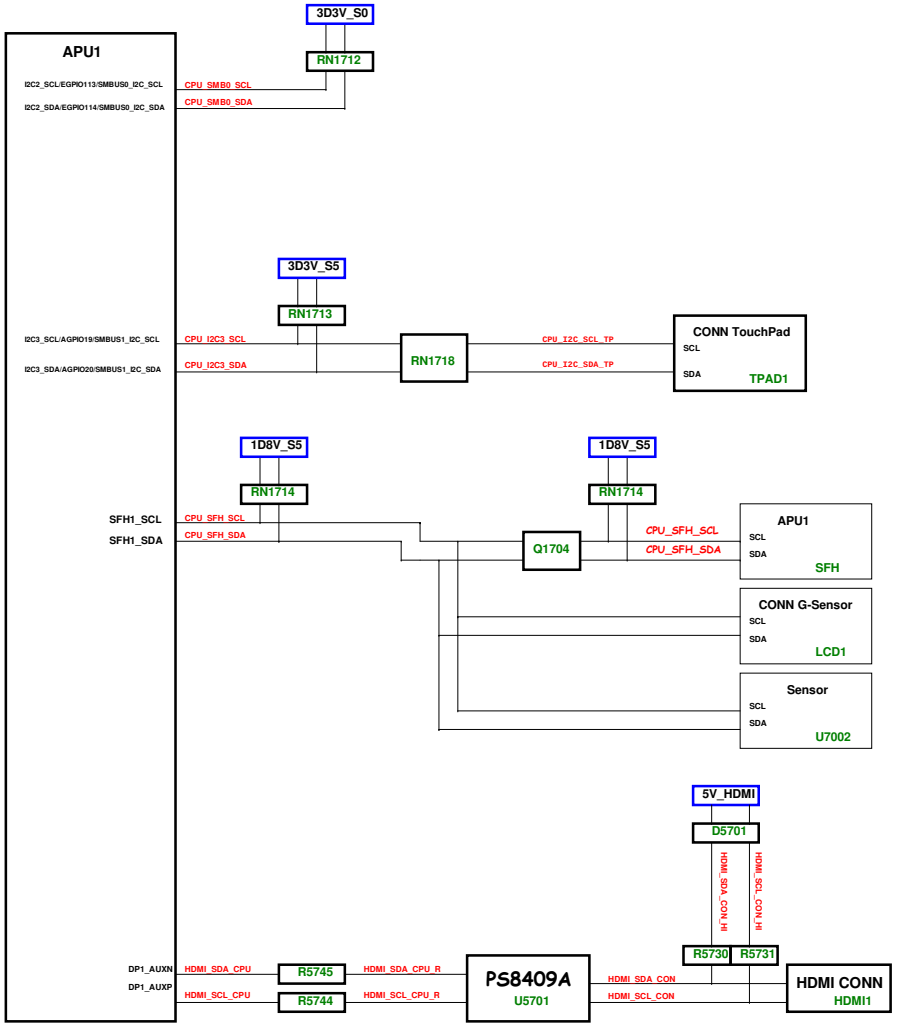
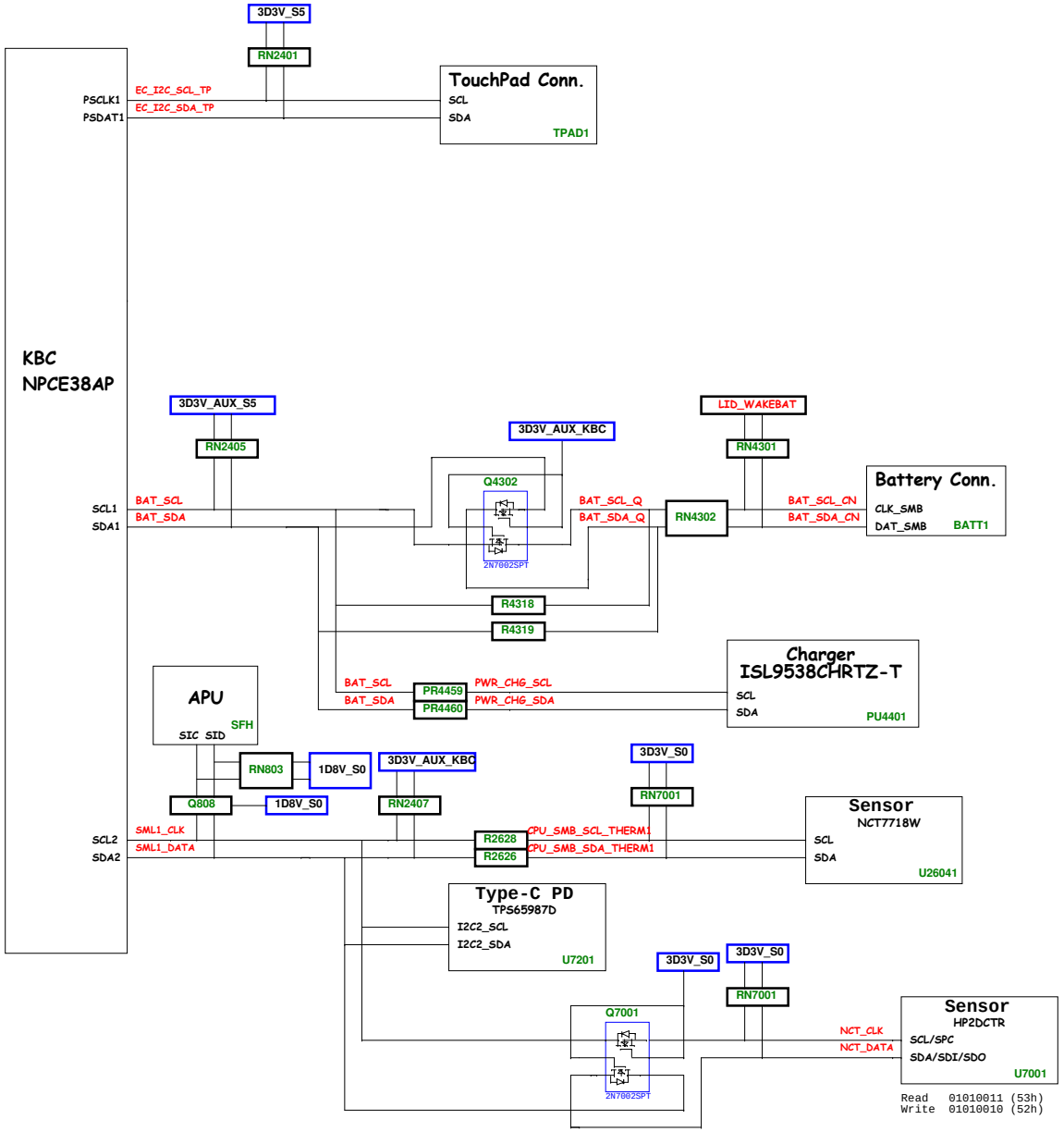
APU SMBus Block Diagram



KBC SMBus Block Diagram



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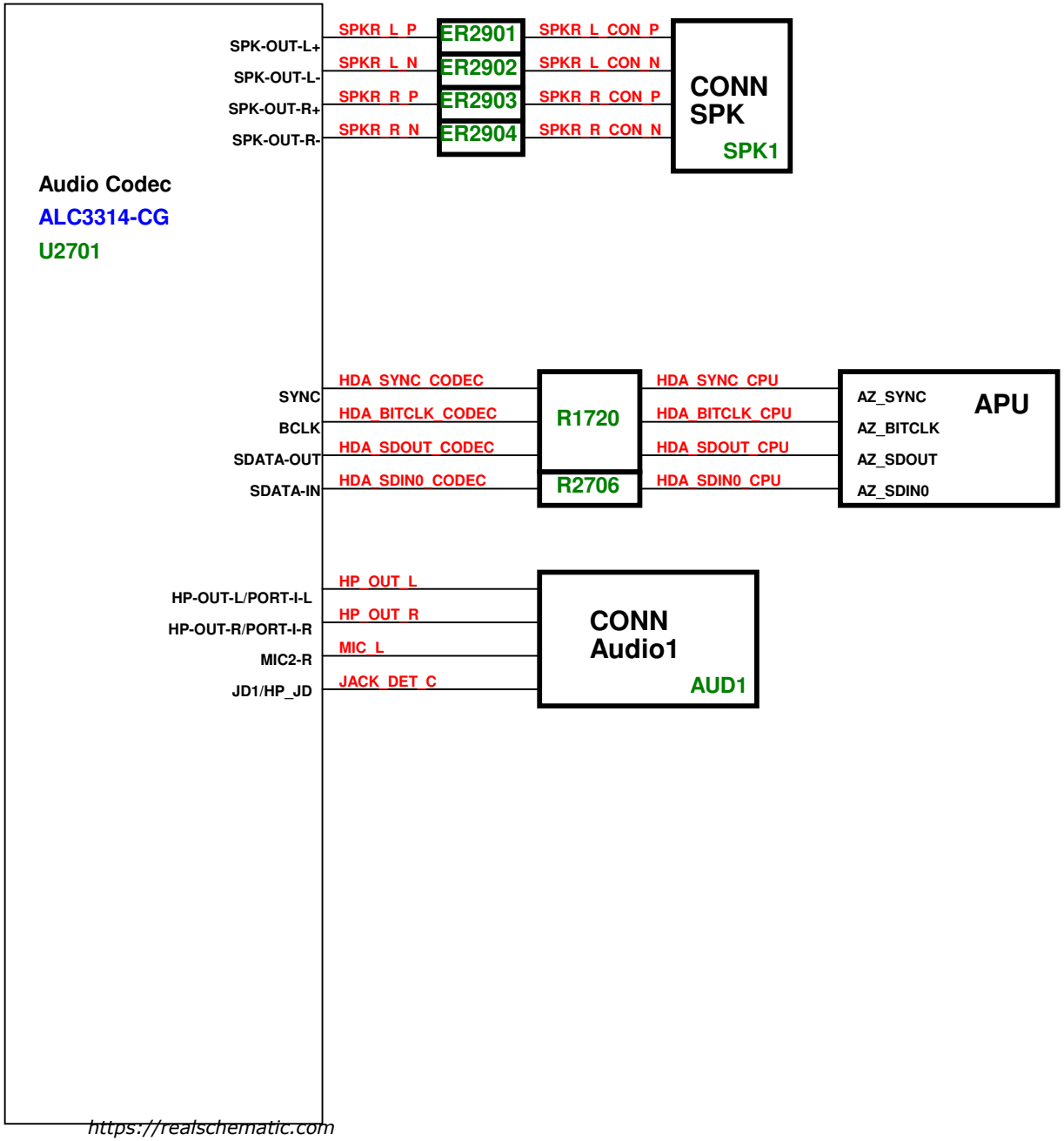
Audio Block Diagram



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